SINGLE-CHIP MICROPROCESSOR DCT11-AA

T11 TECHNICAL NOTE

Features

- Basic PDP-11 Instruction Set (less MARK and EIS/FIS)
- Vectored Interrupts on Four Priority Levels
- 15 Internally Generated Vectors
- Full Dynamic Memory Support
  - —Dynamic Memory Address
  - —RAS and CAS Strobes
  - —Refresh Counter
  - —Automatic Refresh Cycles
- TTL Compatible Signals
- Signal +5 V Power Supply
- Internal Clock Oscillator Circuit
- Bus Compatibility with Most Industry Standard Peripheral Chips
- Programmable Mode Register Featuring:
  - 8- or 16-bit Data Bus
  - Automatic Start/Restart Addresses
  - Static or Dynamic Memory Support
  - Bus Synchronous or Constant Frequency Clock Output
  - Normal or Lengthened Bus Transactions

Description

The DCT11-AA (T11) is Digital Equipment Corporation's PDP-11 single chip microprocessor. Its instruction set is compatible with that of the LSI-11. The DCT11-AA supports most industry standard peripheral chips and can operate at a maximum clock rate of 7.5 megahertz. This powerful microprocessor fully supports both static and dynamic memories.

The DCT11-AA incorporates DMA support as well as an internal and external interrupt structure. The chip uses a time multiplexed address/data bus and a time multiplexed address/interrupt bus.

Through the use of a programmable mode register loaded during power up, the DCT11-AA can be adapted to a wide variety of applications.

Table 1. Characteristics

Maximum Power Dissipation	1.1 Watt
V_{CC}	+5 V (± .25 V)
I_{OL} max @ V_{OL} = .4 V @ C_L 80 pF	3.2 mA
Operating Frequency (max)	7.5 MHz
Ambient Temperature Operating Range	0° to +70° C
Storage Temperature Range	−55° to +125° C

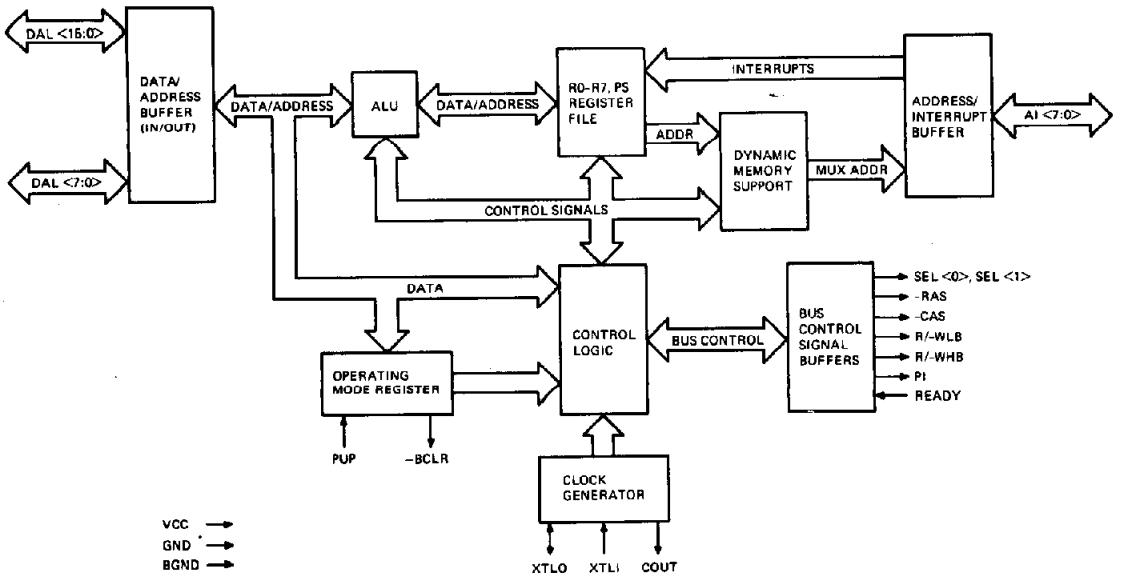

Figure 1. DCT11-AA (T11) Block Diagram

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Table 2. DCT11-AA Pin Functions

Pin No.	Pin Name	Definition	Function
1-7, 9-17	DAL<15:0>	Data/Address Lines	16 BIT MODE DAL<15:0> are multiplexed with address and data during a read/write transaction. 8-BIT MODE DAL<15:8> become Static Address Lines (SAL<15:8>) and contain the high byte of the address during the entire read/write transaction. DAL<7:0> are multiplexed during a read/write transaction and contain first the low byte of address and low byte of data then the low byte of address + 1 and high byte of data. DYNAMIC MODE In dynamic mode, memory addressing is provided simultaneously on DAL<15:0> and AI<7:0>. IACK (Interrupt Acknowledge) DAL<12:8> are used to output the information present on AI<5:1> during an IACK transaction. DAL<7:2> are used to input the external vector during an IACK transaction. DMA OPERATION DAL<15:0> are three-stated during a DMA transaction. BUS NOP DAL<15:0> contain previously latched data during a BUS NOP and refresh transaction. ASPI (Assert Priority In) DAL<15:0> are three-stated during an ASPI transaction. INITIALIZATION DAL<15:8> and <1:0> are read into the mode register on power up and reset instruction.
8	BGND	Ground	Provides reference ground for all lines of the DCT11-AA.
18	– BCLR	Bus Clear	Signal asserted low by processor during the power up sequence and during execution of RESET instruction.
19	PUP	Power Up	Input with low current internal pulldown that is always enabled.
20	GND	Ground	Provides reference power ground on the DCT11-AA.
21	COUT	Clock Output	TTL level clock which operates at constant clock or processor clock depending on the function of mode register bit 0.
22-23	XTL<1:0>	Crystal	External crystal connections to internal clock generator.
24-25	SEL<1:0>	Select	Encoded lines which indicate the transaction being performed.
26	READY	Ready	Signal used to place the DCT11-AA into an idle state during peripheral operations.
27	R/ – WHB	Read/Write High Byte	Signal asserted will implement a write operation in 16-bit mode and a read operation in 8-bit mode.
28	R/ – WLB	Read/Write Low Byte	Signal asserted will implement a write operation in 16- and 8-bit mode.
29	– RAS	Row Address Strobe	System address strobe.
30	– CAS	Column Address Strobe	Address and chip select strobe.
31	PI	Priority In	Priority in Strobe.

Table 2. DCT11-AA Pin Functions (continued)

Pin No.	Pin Name	Definition	Function
32-39	AI<7:0>	Address/Interrupt Lines	1. AI<5:1> are used to input interrupt request. 2. AI<0> is used to input DMA request. 3. AI<7:0> are used to output both row and column address. 4. AI<5> is used as a control signal which indicates whether an external vector will be used. 5. AI<7:0> are used as inputs in static mode and contain previously latched data in dynamic mode during BUS NOP and IACK transactions.
40	V_{cc}	Positive Supply Voltage	Voltage supply for the DCT11-AA.

The DCT11-AA package is a 40-pin ceramic DIP. Its unique adaptability allows the designer to optimize the DCT11-AA to the application. Pin functions are modified by an external register which is accessed by the chip during power up. Selection of either static or dynamic 8- or 16-bit mode determines the functionality of mode dependent pins. These mode dependent pins include DAL<15:8>, AI<7:0>, SEL<1:0>, R/—WHB, R/—WLB and COUT.

DCT11-AA pin functions are described in the preceding table.

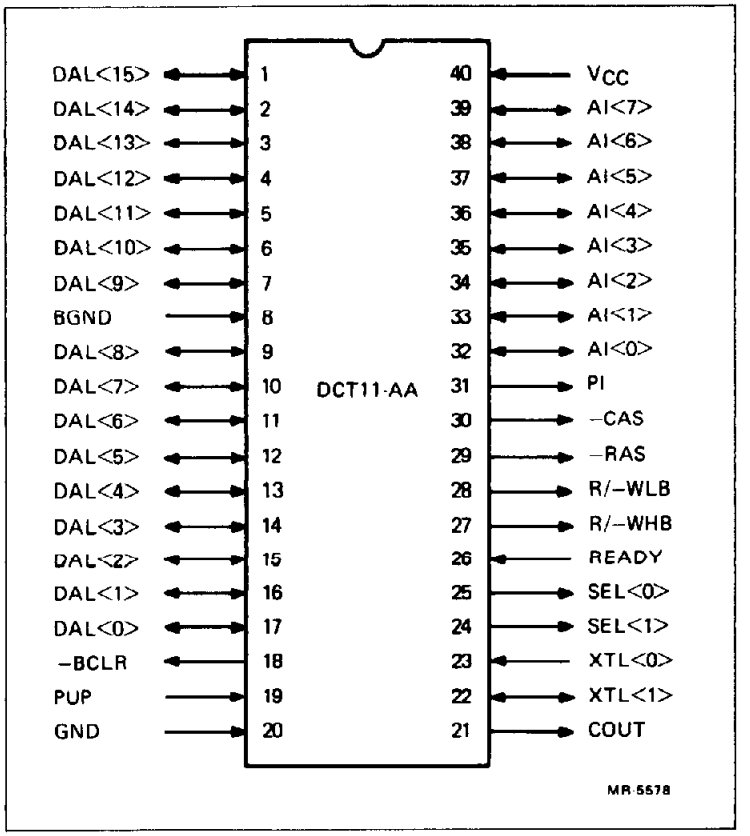
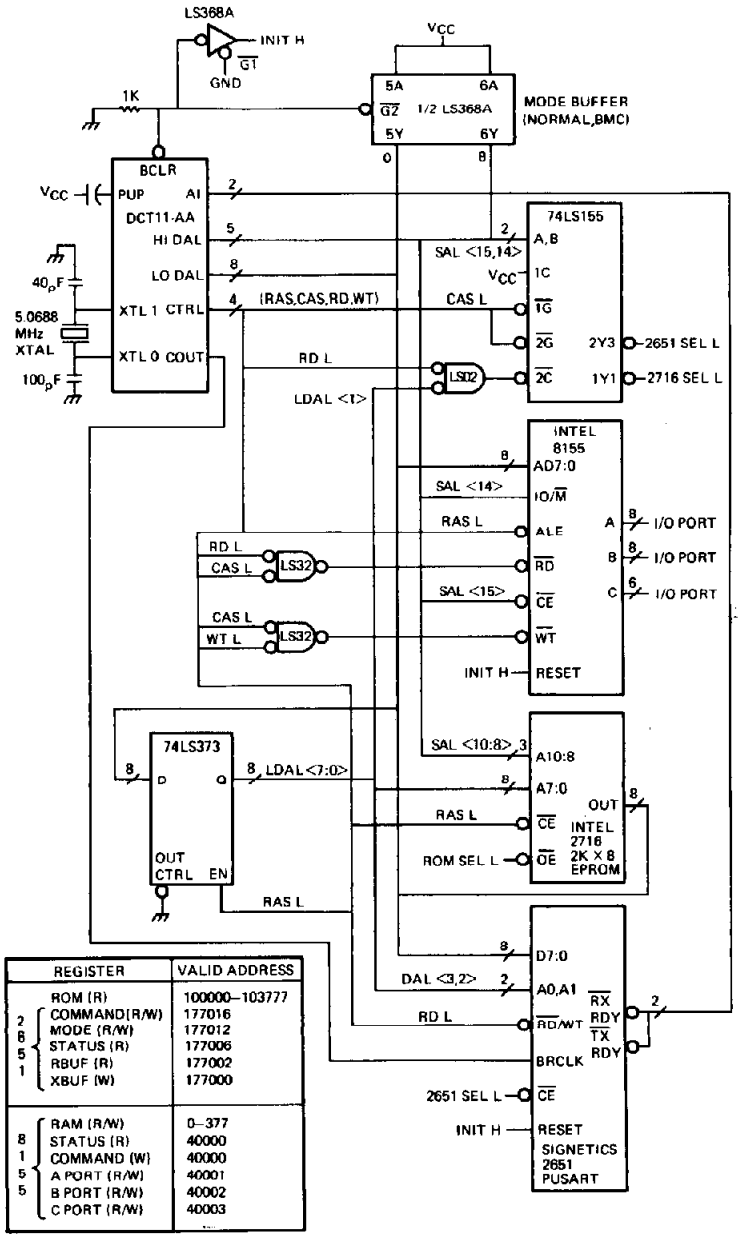


Figure 2. Pin Configuration

The two schematics presented on these pages illustrate the DCT11-AA in an 8-bit and a 16-bit application. Each of these provides a small controller environment. The 16-bit application has a performance approximately 60% greater than that of the 8-bit application. Tradeoffs between performance and complexity are the designer's option.



	REGISTER	VALID ADDRESS
2	ROM (R)	100000–103777
8	COMMAND (R/W)	177016
5	MODE (R/W)	177012
1	STATUS (R)	177006
	RBUF (R)	177002
	XBUF (W)	177000
8	RAM (R/W)	0–377
1	STATUS (R)	40000
5	COMMAND (W)	40000
5	A PORT (R/W)	40001
	B PORT (R/W)	40002
	C PORT (R/W)	40003

NOTE:
2651 MUST BE ACCESSED BY BYTE INSTRUCTIONS ONLY.

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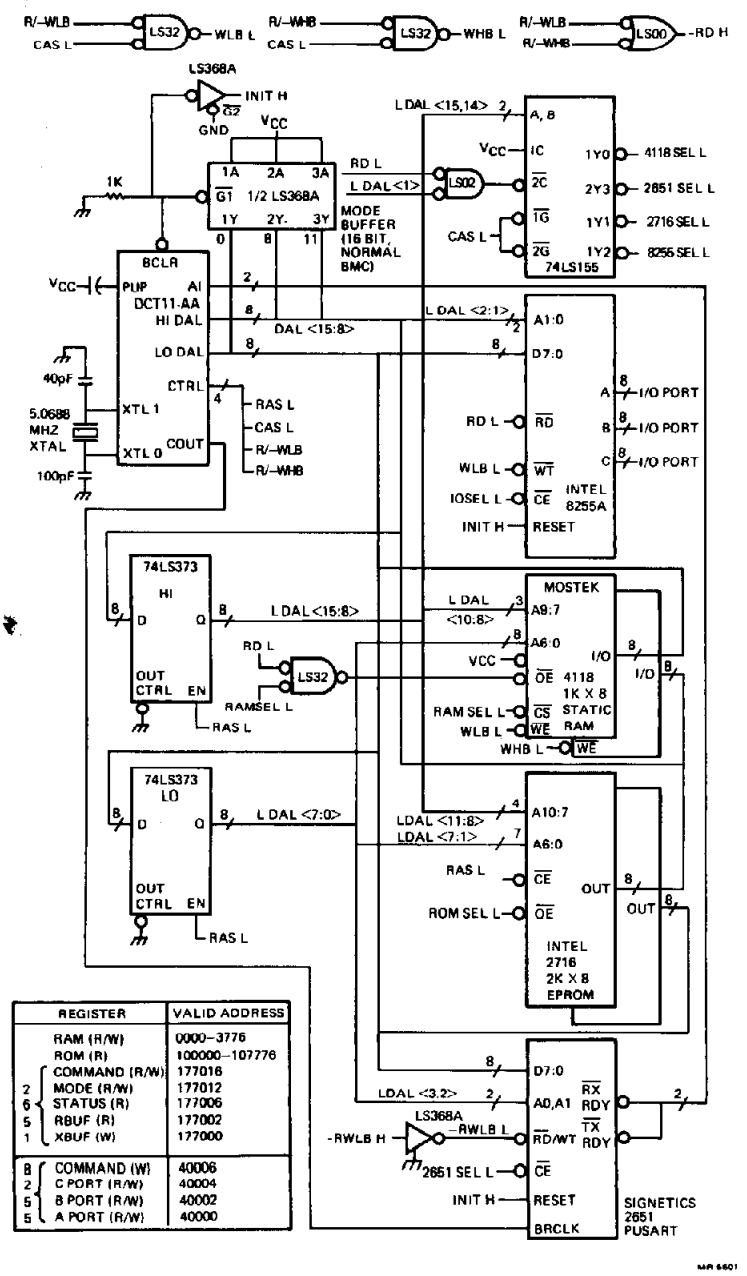
Figure 3. 8-Bit Application



REGISTER		VALID ADDRESS
	RAM (R/W)	0000–3776
	ROM (R)	100000–107776
2	COMMAND (R/W)	177016
6	MODE (R/W)	177012
5	STATUS (R)	177006
1	RBUF (R)	177002
	XBUF (W)	177000
8	COMMAND (W)	40006
2	C PORT (R/W)	40004
5	B PORT (R/W)	40002
5	A PORT (R/W)	40000

Figure 4. 16-Bit Application

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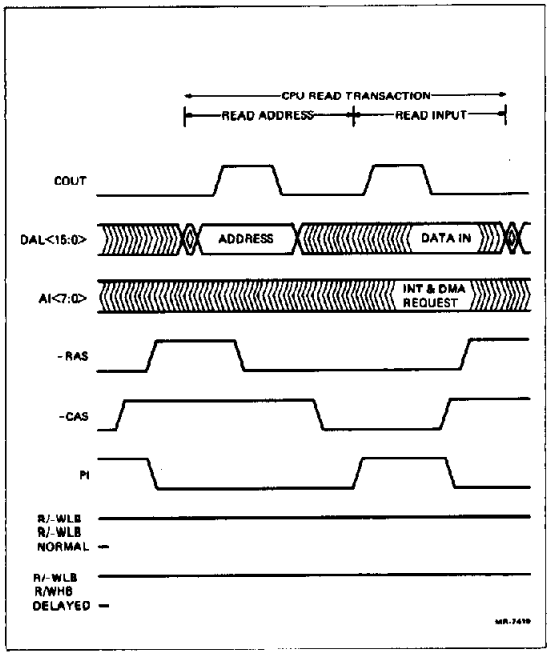

Figure 5. 16-Bit Static Read

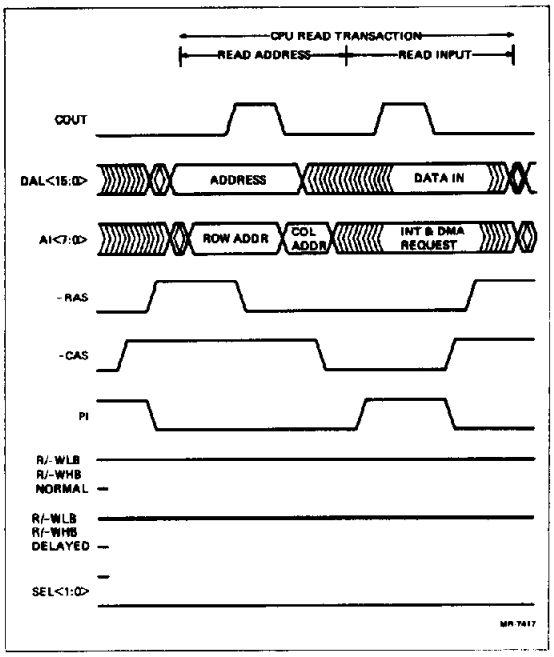

Figure 6. 16-Bit Dynamic Read

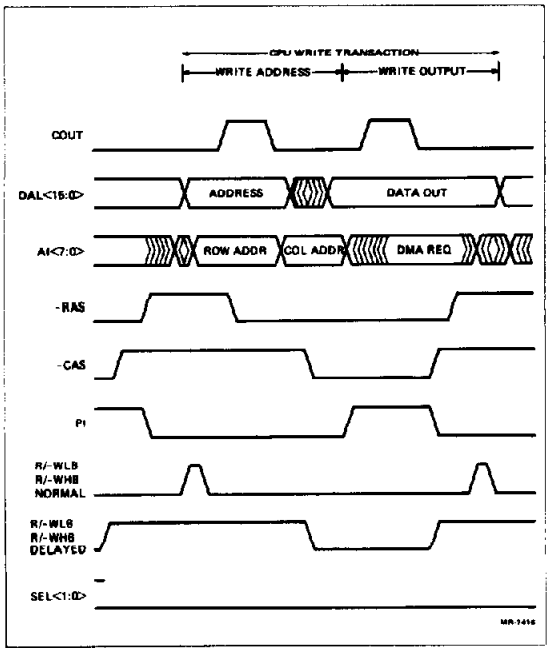

Figure 7. 16-Bit Static Write

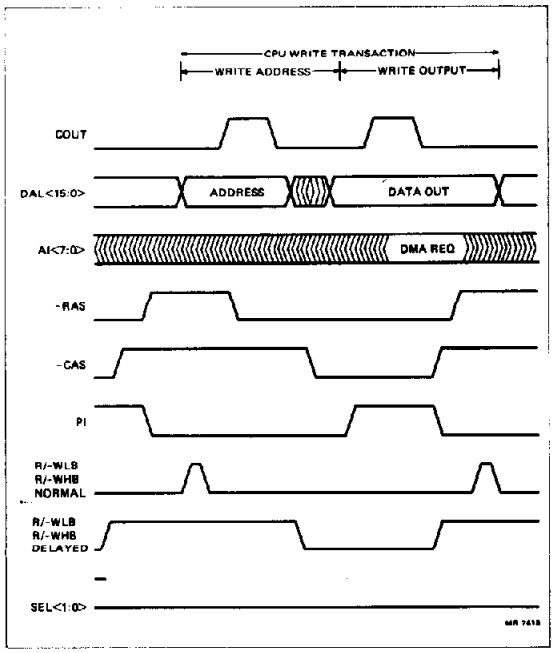

Figure 8. 16-Bit Dynamic Write

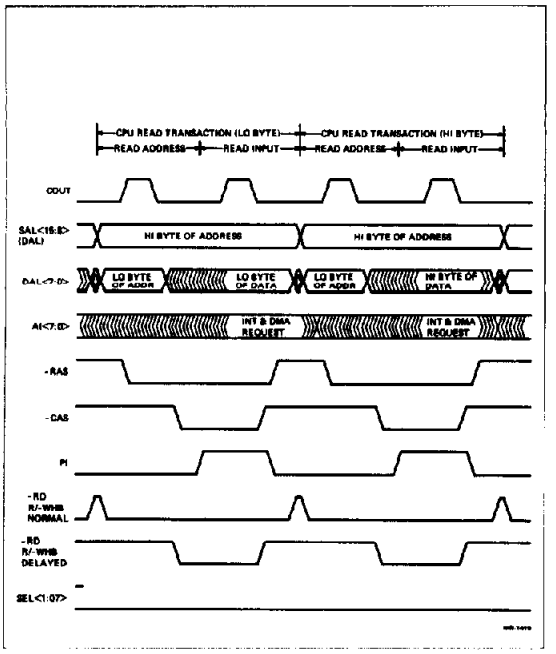

Figure 9. 8-Bit Static Read

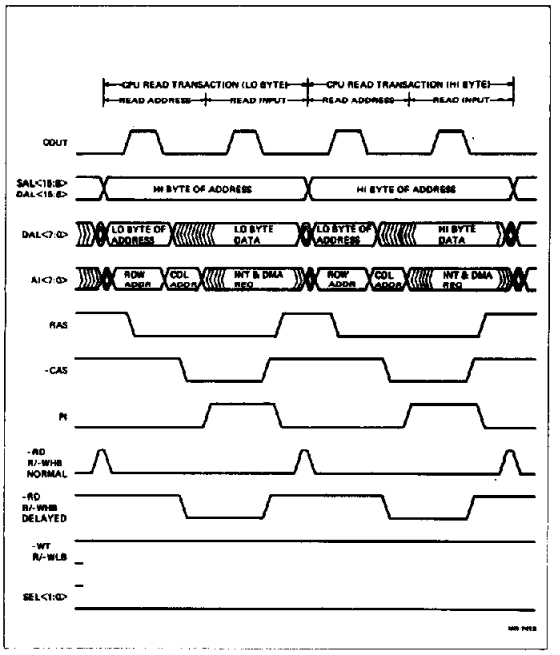

Figure 10. 8-Bit Dynamic Read

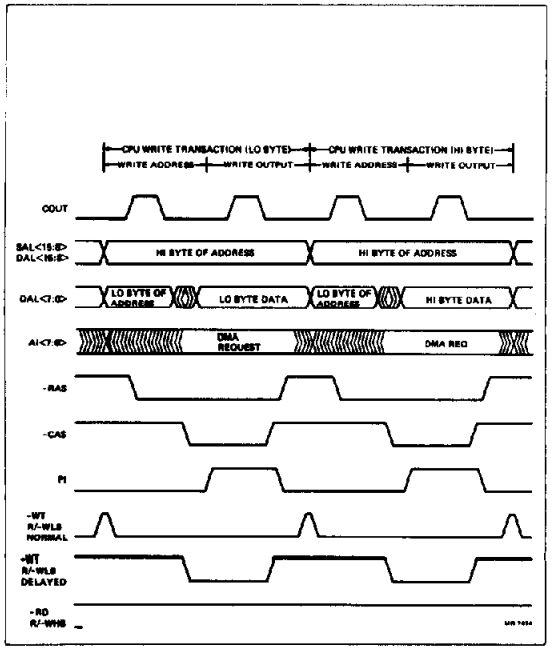

Figure 11. 8-Bit Static Write

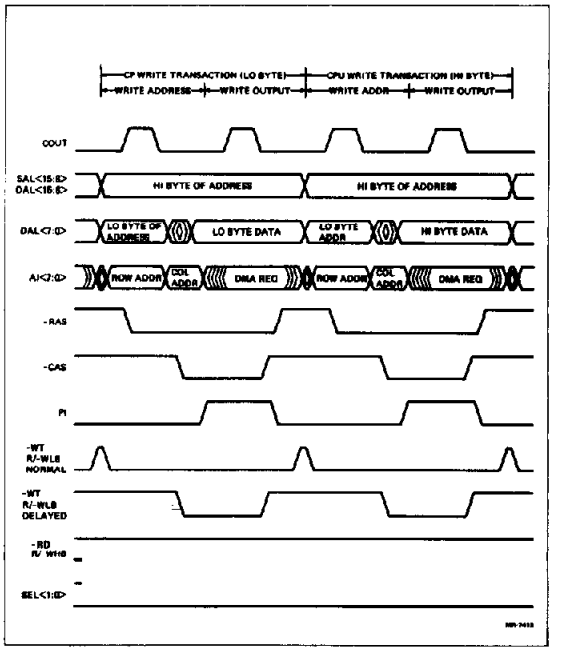

Figure 12. 8-Bit Dynamic Write

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