ZILOG

PRELIMINARY PRODUCT SPECIFICATION

Z89321/371/391

16-BIT DIGITAL SIGNAL PROCESSOR

FEATURES

DSP Core

- 20 MIPS, 16-Bit Fixed Point DSP
- 50 ns Instruction Cycle Time
- Static Architecture
- 512 Word On-Chip RAM
- 4K Word On-Chip Masked Program ROM (Z89321)
- 4K Word One-Time Programmable (Z89371)
- 64K Word External Program ROM (Z89391)
- Modified Harvard Architecture
- Six-Level Hardware Stack
- Six Register Address Pointers
- Optimized Instruction Set (30 Instructions)

On-Board Peripherals

- 8/16-Bit Dual CODEC Interface Capable of up to 10 Mbps
- μ-Law Compression Option (Decompression is performed in software)
- 16-Bit I/O Bus (Tri-Stated)
- Three I/O Address Pins (Latched Outputs)
- Two User Input Pins
- Two User Output Pins
- Wait-State Generator
- Three Vectored Interrupts
- 13-Bit General-Purpose Timer

GENERAL DESCRIPTION

The Z893XX Family is Zilog's first generation CMOS Digital Signal Processors (DSP's). Single cycle instruction execution and a Harvard bus structure promotes efficient algorithm execution. The processor contains a 4K word program ROM and 512 work data RAM. An external 64K word Program Memory Space is available with the Z89391. Six register pointers provide circular buffering capabilities and dual operand fetching. Three vectored interrupts are complemented by a six level stack. The CODEC interface enables high-speed transfer rates to accommodate digital audio and voice data. A dedicated Counter/Timer provides the necessary timing signals for the CODEC interface. An additional 13-bit timer is available for general-purpose use.

The Z893XX DSP's are optimized to accommodate advanced signal processing algorithms. The 20-MIPS operating performance and efficient architecture provides real-time execution. Compression, filtering, frequency detection, audio, voice detection/synthesis and other vital algorithms can all be accommodated. The on-board CODEC interface is compatible with 8-bit PCM and 16-bit CODECs, including Crystal's 4215/4216 for digital audio applications. The wait-state generator integrates flexibility to accommodate slow external peripherals.

Note: When referencing Z89321, topic applies equally to Z89371 and Z89391 unless specified.

GENERAL DESCRIPTION (Continued)

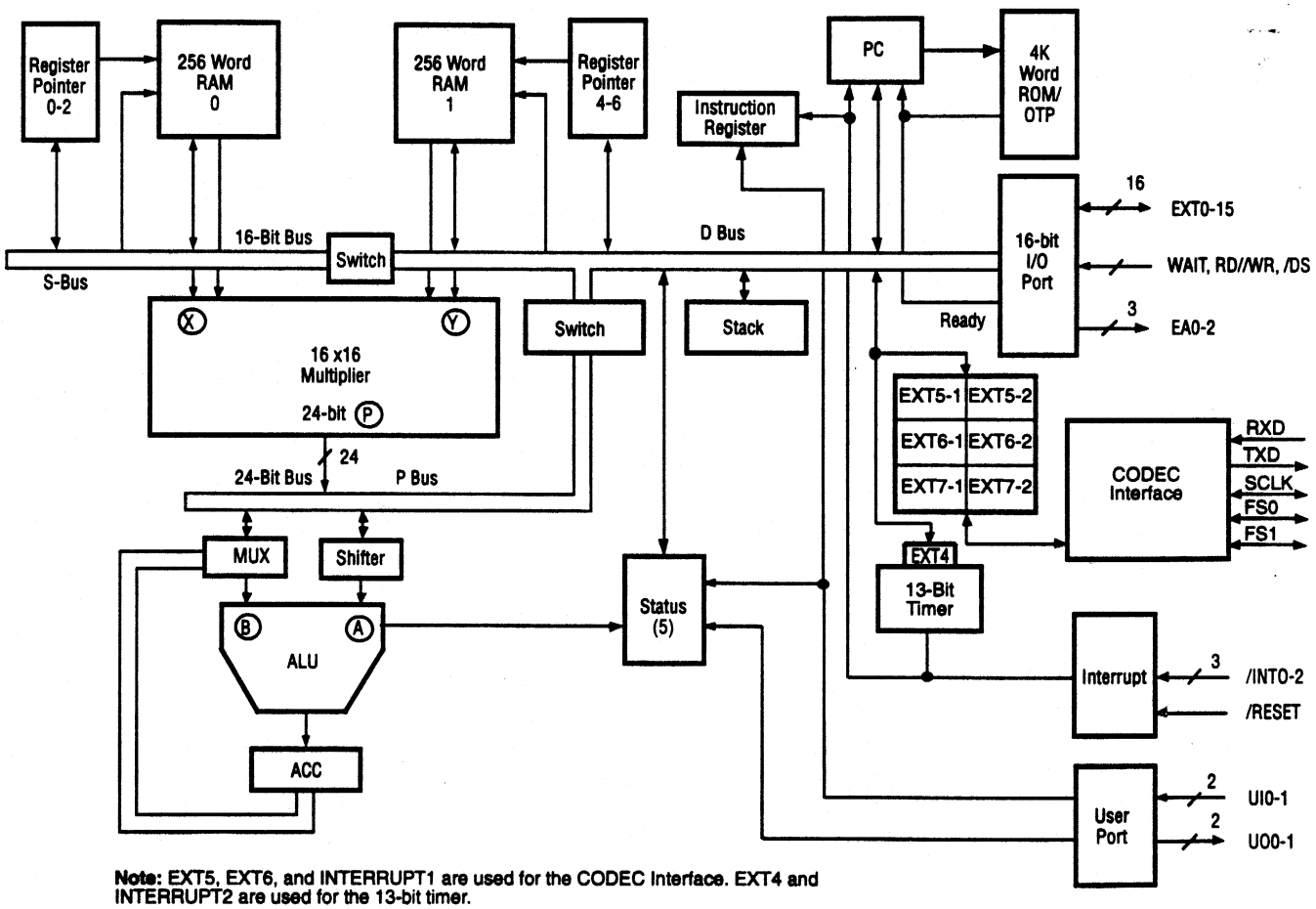
For prototyping purposes, the Z89371 is a one-time programmable (OTP) device with a 16 MHz maximum operating frequency. Package styles for these DSP devices are: 40-pin DIP, 44-pin PLCC, 44-pin QFP for the Z89321/371, and 84-pin PLCC for the Z89391.

Development tools for the IBM PC include a relocatable assembler, a linker loader, and an ANSI-C compiler. Also, the development tools include a cross assembler for the TMS320 family assembly code and a hardware emulator.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

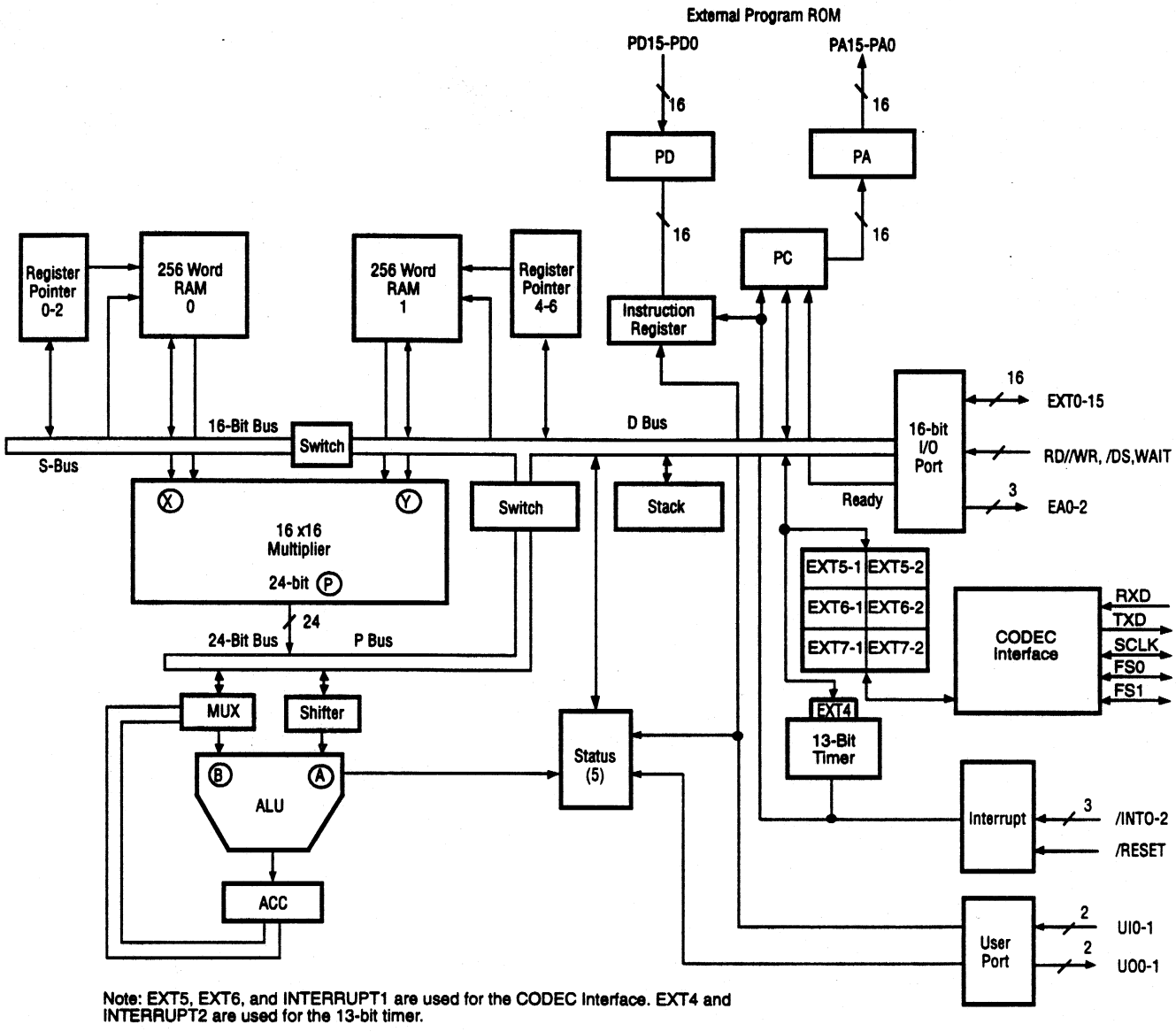
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Note: EXT5, EXT6, and INTERRUPT1 are used for the CODEC Interface. EXT4 and INTERRUPT2 are used for the 13-bit timer.

Figure 1. Z89321/371 Functional Block Diagram



Note: EXT5, EXT6, and INTERRUPT1 are used for the CODEC Interface. EXT4 and INTERRUPT2 are used for the 13-bit timer.

Figure 2. Z89391 Functional Block Diagram

PIN DESCRIPTION

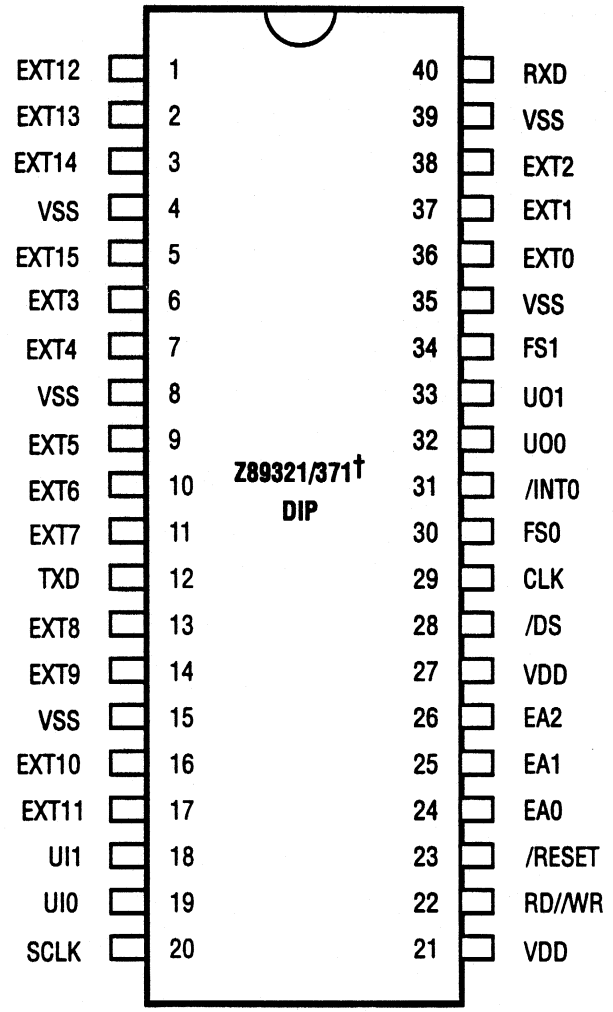


Figure 3. Z89321/371 40-Pin DIP Pin Assignments

Table 1. Z89321/371 40-Pin DIP Pin Identification

No.	Symbol	Function	Direction
1-3	EXT12-EXT14	External data bus	Input/Output
4	V_{SS}	Ground	Input
5	EXT15	External data bus	Input/Output
6-7	EXT3-EXT4	External data bus	Input/Output
8	V_{SS}	Ground	Input
9-11	EXT5-EXT7	External data bus	Input/Output
12	TXD	Serial output to CODECs	Output
13-14	EXT8-EXT9	External data bus	Input/Output
15	V_{SS}	Ground	Input
16-17	EXT10-EXT11	External data bus	Input/Output
18	UI1	User input	Input
19	UI0	User input	Input
20	SCLK	Codec serial clock	Input/Output*
21	V_{DD}	Power Supply	Input
22	RD//WR	Strobes for external bus	Output
23	/RESET	Reset	Input
24-26	EA0-EA2	External address bus	Output
27	V_{DD}	Power Supply	Input
28	/DS	Data strobe for external bus	Output
29	CLK	Clock	Input
30	FS0	Codec 0 Frame Sync	Input/Output*
31	/INT0	Interrupt	Input
32-33	UO0-UO1	User output	Output
34	FS1	Codec 1 Frame Sync	Input/Output*
35	V_{SS}	Ground	Input
36-38	EXT0-EXT2	External data bus	Input/Output
39	V_{SS}	Ground	Input
40	RXD	Serial Input from Codecs	Input

Notes:
* Defined input or output by interface mode selection.
† 40-pin DIP option does not provide HALT and WAIT pins.

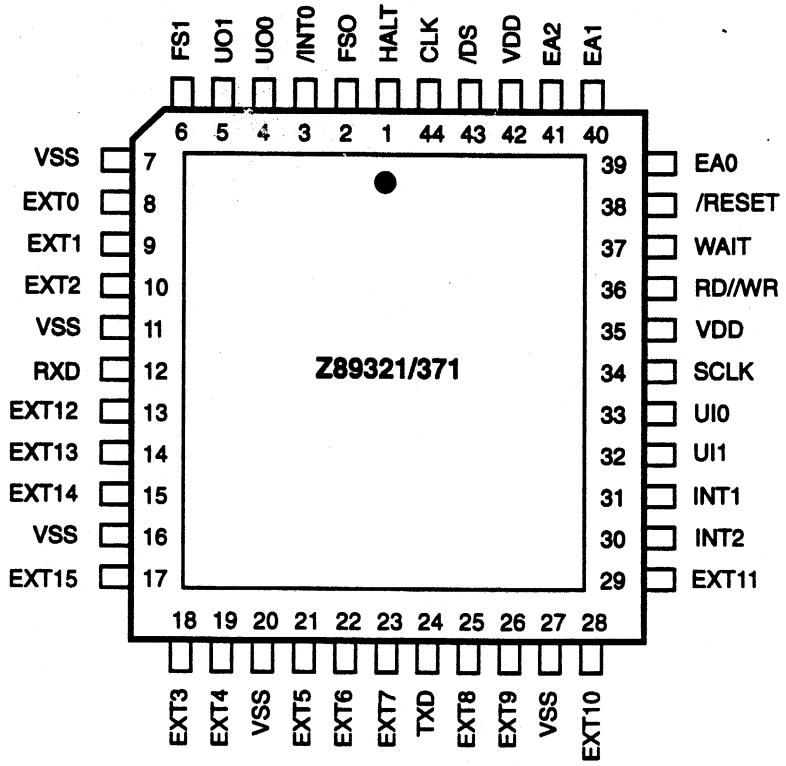


Figure 4. Z89321/371 44-Pin PLCC Pin Assignments

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
1	HALT	Stop execution	Input
2	FS0	CODEC 0 Frame Sync	Input/Output*
3	/INT0	Interrupt	Input
4-5	UO0-UO1	User output	Output
6	FS1	CODEC 1 Frame Sync	Input/Output*
7	V_{SS}	Ground	Input
8-10	EXT0-EXT2	External data bus	Input/Output
11	V_{SS}	Ground	Input
12	RXD	Serial Input from CODECs	Input
13-15	EXT12-EXT14	External data bus	Input/Output
16	V_{SS}	Ground	Input
17	EXT15	External data bus	Input/Output
18-19	EXT3-EXT4	External data bus	Input/Output
20	V_{SS}	Ground	Input
21-23	EXT5-EXT7	External data bus	Input/Output
24	TXD	Serial output to CODECs	Output
25-26	EXT8-EXT9	External Data Bus	Input/Output
27	V_{SS}	Ground	Input
28-29	EXT10-EXT11	External data bus	Input/Output
30	/INT2	Interrupt	Input
31	/INT1	Interrupt	Input
32	UI1	User input	Input
33	UI0	User input	Input
34	SCLK	CODEC serial clock	Input/Output*
35	V_{DD}	Power Supply	Input
36	RD//WR	RD//WR Strobe for EXT Bus	Output
37	WAIT	WAIT State	Input
38	/RESET	Reset	Input
39-41	EA0-EA2	External address bus	Output
42	V_{DD}	Power Supply	Input
43	/DS	Data strobe for external bus	Output
44	CLK	Clock	Input

Note:
* Defined input or output by interface mode selection.

PIN DESCRIPTION (Continued)

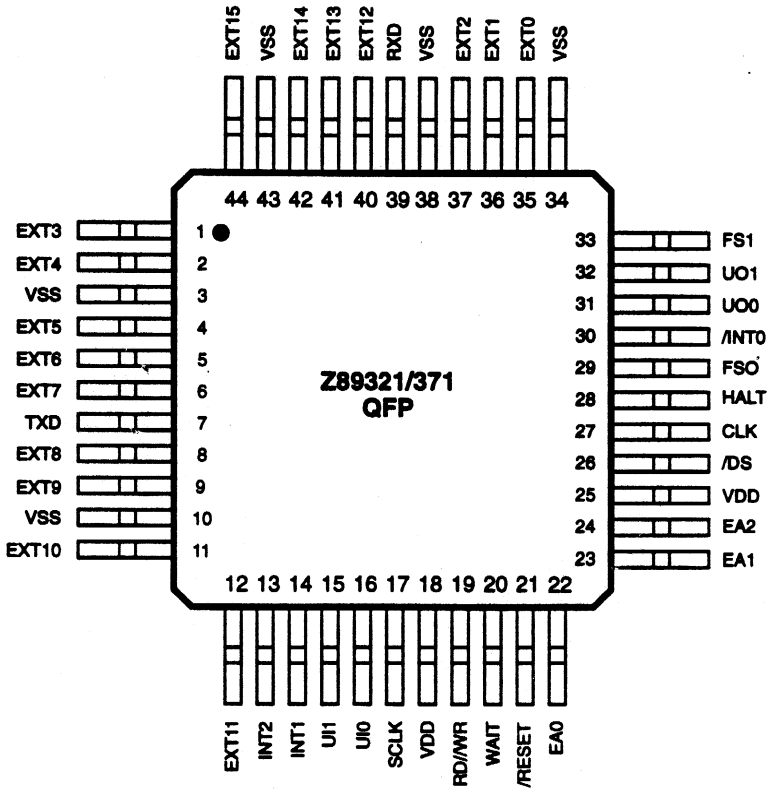


Figure 5. Z89321/371 44-Pin QFP Pin Assignments

Table 3. Z89321/371 44 in QFP Pin Identification

No.	Symbol	Function	Direction
1-2	EXT3-EXT4	External data bus	Input/Output
3	V_{SS}	Ground	Input
4-6	EXT5-EXT7	External data bus	Input/Output
7	TXD	Serial output to CODECs	Output
8-9	EXT8-EXT9	External Data Bus	Input/Output
10	V_{SS}	Ground	Input
11-12	EXT10-EXT1	External Data Bus	Input/Output
13	/INT2	Interrupt	Input
14	/INT1	Interrupt	Input
15	UI1	User Input	Input
16	UI0	User Input	Input
17	SCLK	CODEC Serial Clock	Input/Output*
18	V_{DD}	Power Supply	Input
19	RD//WR	RD//WR Strobe EXT Bus	Output
20	WAIT	WAIT State	Input
21	/RESET	Reset	Input
22-24	EA0-EA2	External Address Bus	Output
25	V_{DD}	Power Supply	Input
26	/DS	Data Strobe for External Bus	Output
27	CLK	Clock	Input
28	HALT	Stop execution	Input
29	FS0	CODEC 0 Frame Sync	Input/Output*
30	/INT0	Interrupt	Input
31-32	UO0-UO1	User output	Output
33	FS1	CODEC 1 Frame Sync	Input/Output*
34	V_{SS}	Ground	Input
35-37	EXT0-EXT2	External data bus	Input/Output
38	V_{SS}	Ground	Input
39	RXD	Serial input to CODECs	Input
40-42	EXT12-EXT14	External Data Bus	Input/Output
43	V_{SS}	Ground	Input
44	EXT15	External Data Bus	Input/Output

Note:
* Defined input or output by interface mode selection.

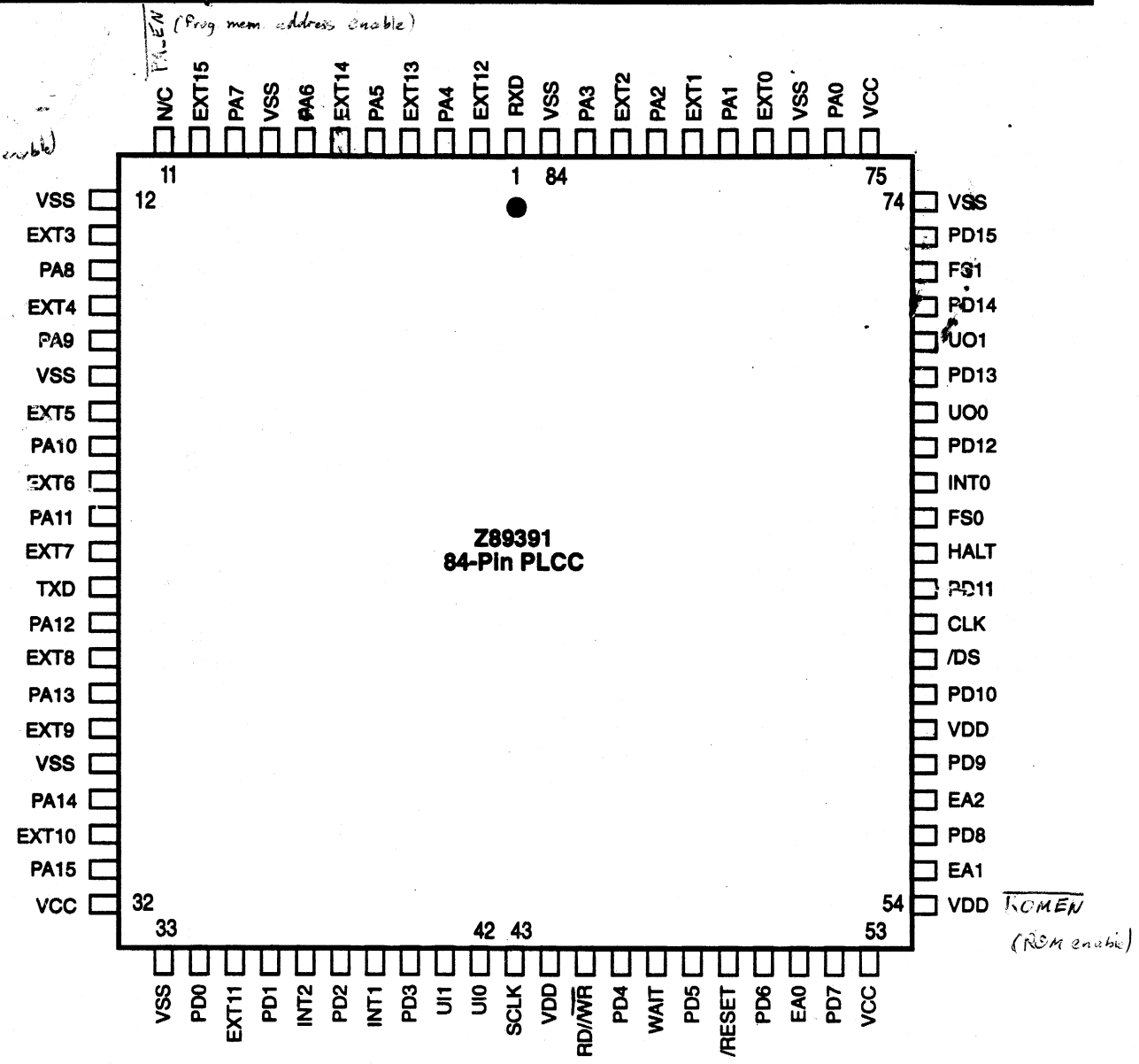


Figure 6. Z89391 84-Pin PLCC Pin Assignments

PIN DESCRIPTION (Continued)

Table 4. Z89391 84-Pin PLCC Pin Identification

Symbol	Function	Direction
EXT15-EXT0	External data bus	Input/Output
V_{SS}	Ground	Input
PD15-PD0	Program data bus	Input
PA15-PA0	Program address bus	Output
V_{DD}	Power Supply	Input
EA2-EA0	External address bus	Output
/DS	Data Strobe	Output
RD//WR	READ//WRITE Strobe	Output
WAIT	WAIT State	Input
/RESET	Reset	Input
CLK	Clock	Input
HALT	Stop execution	Input
UI1-UI0	User inputs	Input
INT2-INT0	Interrupts	Input
UO1-UO0	User outputs	Output
SCLK	CODEC Serial Clock	Input/Output*
FS0	CODEC 0 Frame Sync	Input/Output*
FS1	CODEC 1 Frame Sync	Input/Output*
RXD	Serial input to CODECs	Input
TXD	Serial output to CODECs	Output

* Defined input or output mode by interface mode selection

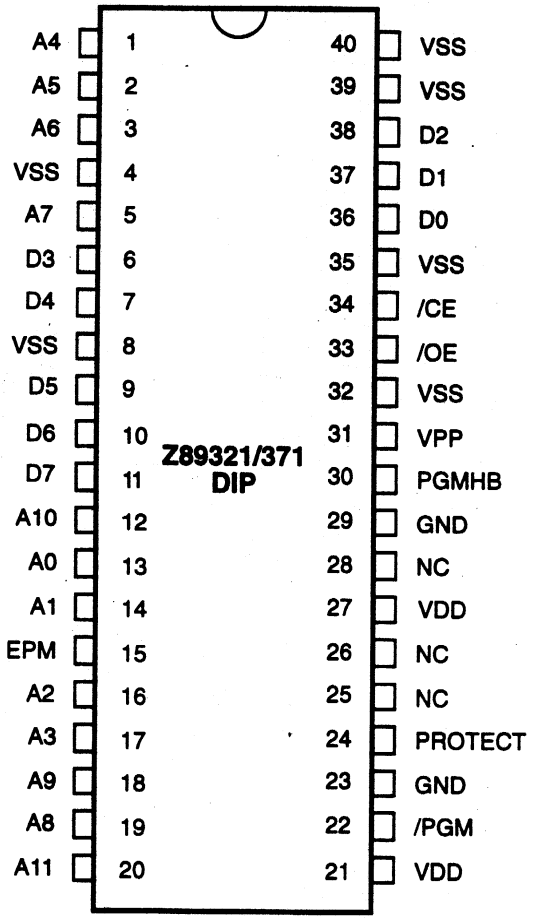


Figure 7. Z89321/371 40-Pin DIP Pin Assignments (EPROM Mode)

Table 5. Z89321/371 40-Pin DIP Pin Identification (EPROM Mode)

No.	Symbol	Function	Direction
1-3	A4-A6	Address 4-6	Input
4	V_{SS}	Ground	Input
5	A7	Address 7	Input
6-7	D3-D4	Data 3,4	Input
8	V_{SS}	Ground	Input
9-11	D5-D7	Data 5,6,7	Input/Output
12	A10	Address 10	Input
13-14	A0-A1	Address 0,1	Input
15	EPM	Programming Mode	Input
16-17	A2-A3	Address 2,3	Input
18	A9	Address 9	Input
19	A8	Address 8	Input
20	A11	Address 11	Input
21	V_{DD}	Power Supply	Input
22	PGM	EPROM Programming	Input
23	V_{SS}	Ground	Input
24	Protect	EPROM Protect	Input
25-26	V_{SS}	Ground	Input
27	V_{DD}	Power Supply	Input
28	N/C	No Connection	
29	V_{SS}	Ground	Input
30	PGMHB	Program High Byte	Input
31	VPP	Program Voltage	Input
32	N/C	No Connection	
33	/OE	Output Enable	Input
34	/CE	Chip Select	Input
35	V_{SS}	Ground	Input
36-38	D0-D2	Data 0,1,2	Input/Output
39	V_{SS}	Ground	Input
40	V_{SS}	Ground	Input

PIN DESCRIPTION (Continued)

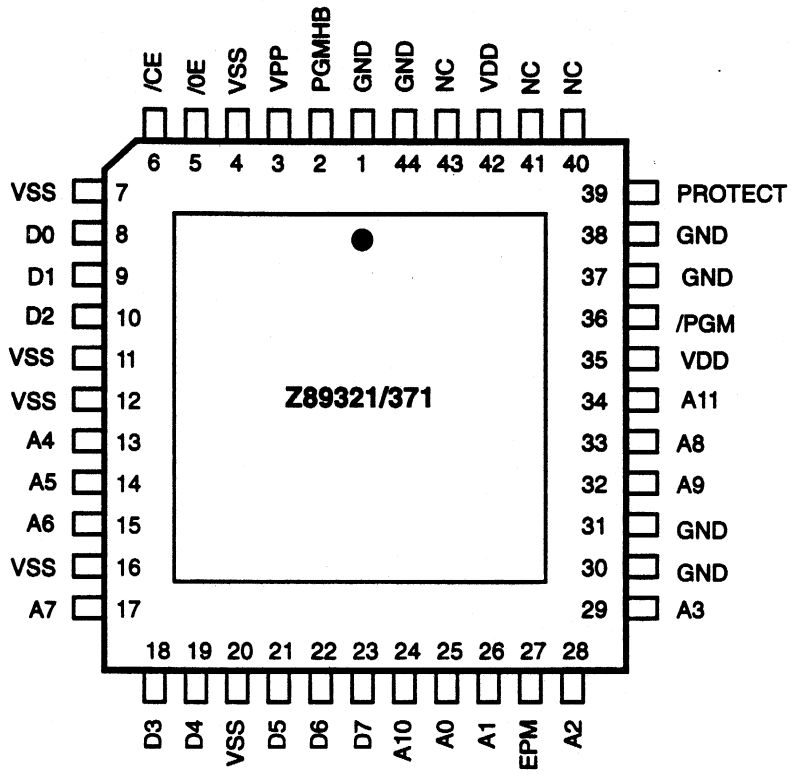


Figure 8. Z89321/371 44-Pin PLCC Pin Assignments (EPROM Mode)

Table 6. Z89321/371 44-Pin PLCC Pin Identification (EPROM Mode)

No.	Symbol	Function	Direction
1	V_{SS}	Ground	Input
2	PGMHB	Program High Byte	Input
3	V_{PP}	Program Voltage	Input
4	V_{SS}	Ground	Input
5	/OE	Output Enable	Input
6	/CE	Chip Select	Input
7	V_{SS}	Ground	Input
8-10	D0-D2	Data 0,1,2	Input
11	V_{SS}	Ground	Input
12	V_{SS}	Ground	Input
13-15	A4-A6	Address 4,5,6	Input
16	V_{SS}	Ground	Input
17	A7	Address 7	Input
18-19	D3-D4	Data 3,4	Input/Output
20	V_{SS}	Ground	Input
21-23	D5-D7	Data 5,6,7	Input/Output
24	A10	Serial output to CODECs	Output
25-26	A0-A1	Address 0,1	Input
27	EPM	Programming Mode	Input
28-29	A2-A3	Address 2,3	Input
30	V_{SS}	Ground	Input
31	V_{SS}	Ground	Input
32	A9	Address 9	Input
33	A8	Address 8	Input
34	A11	Address 11	Input
35	V_{DD}	Power Supply	Input
36	/PGM	EPROM Programming	Input
37	V_{SS}	Ground	Input
38	V_{SS}	Ground	Input
39	Protect	EPROM Protect	Input
40-41	N/C	No Connection	
42	V_{DD}	Power Supply	Input
43	N/C	No Connection	
44	V_{SS}	Ground	Input

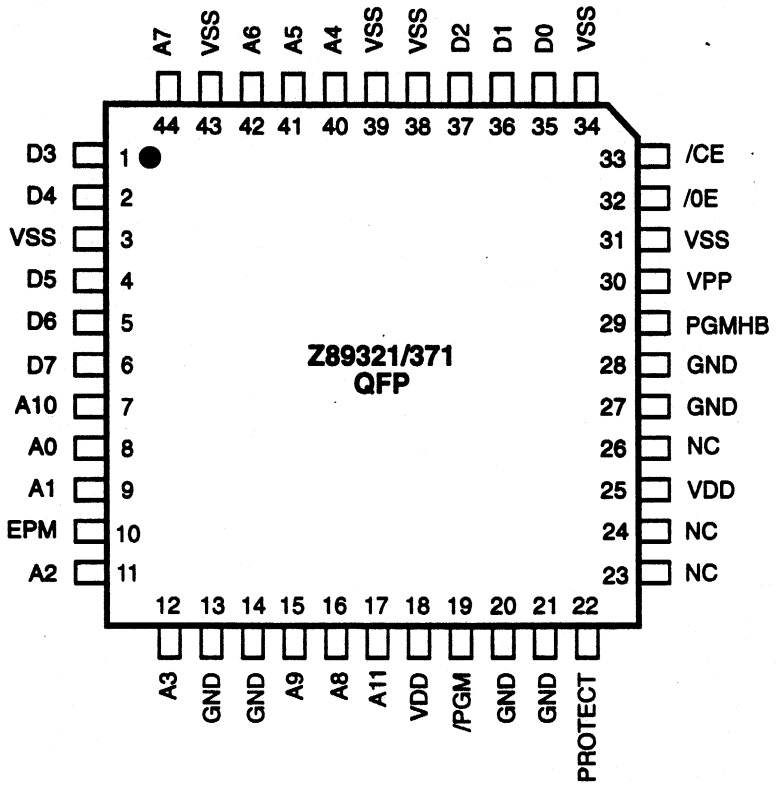


Figure 9. Z89321/371 44-Pin QFP Pin Assignments (EPROM Mode)

Table 7. Z89321/371 44-Pin QFP Pin Identification (EPROM Mode)

No.	Symbol	Function	Direction	No.	Symbol	Function	Direction
1-2	D3-D4	Data 3,4	Input/Output	23-24	N/C	No Connection	
3	V_{SS}	Ground	Input	25	V_{DD}	Power Supply	Input
4-6	D5-D7	Data 5,6,7	Input/Output	26	N/C	No Connection	
7	A10	Serial output to CODECs	Output	27	V_{SS}	Ground	Input
8-9	A0-A1	Address 0,1	Input	28	V_{SS}	Ground	Input
10	EPM	Programming Mode	Input	29	PGMHB	Program High Byte	Input
11-12	A2-A3	Address 2,3	Input	30	V_{PP}	Program Voltage	Input
13	V_{SS}	Ground	Input	31	V_{SS}	Ground	Input
14	V_{SS}	Ground	Input	32	/OE	Output Enable	Input
15	A9	Address 9	Input	33	/CE	Chip Select	Input
16	A8	Address 8	Input	34	V_{SS}	Ground	Input
17	A11	Address 11	Input	35-37	D0-D2	Data 0,1,2	Input
18	V_{DD}	Power Supply	Input	38	V_{SS}	Ground	Input
19	/PGM	EPROM Programming	Input	39	V_{SS}	Ground	Input
20	V_{SS}	Ground	Input	40-42	A4-A6	Address 4,5,6	Input
21	V_{SS}	Ground	Input	43	V_{SS}	Ground	Input
22	Protect	EPROM Protect	Input	44	A7	Address 7	Input

PIN FUNCTIONS

CK *Clock* (input). External clock.

EXT15-EXT0 *External Data Bus* (input/output). Data bus for user defined outside registers such as an ADC or DAC. The pins are normally tri-stated except when the outside registers are specified as destination registers in the instructions. All the control signals exist to allow a read or a write through this bus.

RD/WR *Read/Write Strobe* (output). Data direction signal for EXT-Bus. Data is available from the CPU on EXT15-EXT0 when this signal is Low. EXT-Bus is in input mode (high-impedance) when this signal is High.

EA2-EA0 *External Address* (output). User-defined register address output (latched). One of eight user-defined external registers is selected by the processor with these address pins for read or write operations. Since the addresses are part of the processor memory map, the processor is simply executing internal reads and writes. External Addresses EXT4-EXT7 are used internally by the processor if the CODEC interface and 13-bit timer are enabled.

/DS *Data Strobe* (output). Data Strobe signal for EXT-Bus. Data is read by the external peripheral on the rising edge of /DS. Data is read by the processor on the rising edge of CK /DS.

HALT *Halt State (input).* Stop Execution Control. The CPU continuously executes NOPs and the program counter remains at the same value when this pin is held High. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT. (HALT is not provided on the 40-Pin DIP.)

/INT2-/INT0 *Three Interrupts* (input, active Low). Interrupt request 2-0. Interrupts are generated on the rising edge of the input signal. Interrupt vectors for the interrupt service starting address are stored in the program memory locations 0FFFH for /INT0, 0FFEH for /INT1, and 0FFDH for /INT2. Priority is: INT2 = lowest, INT0 = highest. INT1 is dedicated to the CODEC interface and INT2 is dedicated to the 13-bit timer if both peripherals are enabled. (INT1 and 2 pins are not bonded out on the 40-pin DIP.)

/RESET *Reset* (input, active Low). Asynchronous reset signal. The /RESET signal must be kept Low for at least one clock cycle. The CPU pushes the contents of the PC onto the stack and then fetches a new Program Counter (PC) value from program memory address 0FFCH after the reset signal is released.

WAIT *WAIT State* (input). The wait signal is sampled at the rising edge of the clock with appropriate setup and hold times. The normal write cycle will continue when wait is inactive on a rising clock. A single wait-state can be generated internally by setting the appropriate bits in the EXT7-2 register. (/WAIT pin is not provided on the 40-pin DIP.)

UI1-UI0 *Two Input Pins* (input). General-purpose input pins. These input pins are directly tested by the conditional branch instructions. These are asynchronous input signals that have no special clock synchronization requirements.

UO1-UO0 *Two Output Pins* (output). General-purpose output pins. These pins reflect the value of two bits in the status register S5 and S6. These bits have no special significance and may be used to output data by writing to the status register. A mask option is provided for open-drain or push-pull outputs. **Note:** The user output value is the inverse of the status register content.

ADDRESS SPACE

Program Memory. Programs of up to 4K words can be masked into internal ROM (OTP for Z89371). Four locations are dedicated to the vector address for the three interrupts (0FFDH-0FFFH) and the starting address following a Reset (0FFCH). Internal ROM is mapped from 0000H to 0FFFH, and the highest location for program is 0FFBH. A 64K word External Program Memory Space is available on the Z89391.

Internal Data RAM. The Z89321,371 and 391 all have internal 512 x 16-bit word data RAM organized as two banks of 256 x 16-bit words each, referred to as RAM0 and RAM1. Each data RAM bank is addressed by three pointers, referred to as Pn:0 (n = 0-2) for RAM0 and Pn:1 (n = 0-2) for RAM1. The RAM addresses for RAM0 and RAM1 are arranged from 0-255 and 256-511 respectively. The address pointers, which may be written to or read from, are 8-bit registers connected to the lower byte of the internal 16-bit D-Bus and are used to perform modulo addressing. Three addressing modes are available to access the Data RAM: register indirect, direct addressing, and short form direct. These modes are discussed in detail later. The contents of the RAM can be read or written in one machine cycle per word without disturbing any internal registers or status other than the RAM address pointer used for each RAM. The contents of each RAM can be loaded simultaneously into the X and Y inputs of the multiplier.

Registers. The Z89321 has 19 internal registers and up to an additional eight external registers. The external registers are user definable for peripherals such as A/D or D/A or to DMA or other addressing peripherals. External registers are accessed in one machine cycle the same as internal registers.

FUNCTIONAL DESCRIPTION

General. The Z89321 is a high-performance Digital Signal Processor with a modified Harvard-type architecture with separate program and data memory. The design has been optimized for processing power and minimizing silicon space.

Instruction Timing. Most instructions are executed in one machine cycle. Long immediate instructions and Jump or Call instructions are executed in two machine cycles. A multiplication or multiplication/accumulate instruction requires a single cycle. The instruction description's section describes specific instruction cycle times.

The Instruction Descriptions section describes cycle times.

Multiply/Accumulate. The multiplier can perform a 16-bit x 16-bit multiply or multiply accumulate in one machine cycle using the Accumulator and/or both the X and Y inputs. The multiplier produces a 32-bit result, however, only the 24 most significant bits are saved for the next instruction or accumulation. For operations on very small numbers where the least significant bits are important, the data should first be scaled by eight bits (or the multiplier and multiplicand by four bits each) to avoid truncation errors. Note that all inputs to the multiplier should be fractional two's complement 16-bit binary numbers. This puts them in the range [–1 to 0.9999695], and the result is in 24 bits so that the range is [–1 to 0.9999999]. In addition, if 8000H is loaded into both X and Y registers, the resulting multiplication is considered an illegal operation as an overflow would result. Positive one cannot be represented in fractional notation, and the multiplier will actually yield the result 8000H x 8000H = 8000H (–1 x –1 = –1).

ALU. The ALU has two input ports, one of which is connected to the output of the 24-bit Accumulator. The other input is connected to the 24-bit P-Bus, the upper 16 bits of which are connected to the 16-bit D-Bus. A shifter between the P-Bus and the ALU input port can shift the data by three bits right, one bit right, one bit left or no shift.

Hardware Stack. A six-level hardware stack is connected to the D-Bus to hold subroutine return addresses or data. The Call instruction pushes PC+2 onto the stack. The RET instruction pops the contents of the stack to the PC.

User Inputs. The Z89321 has two inputs, UI0 and UI1, which may be used by Jump and Call instructions. The Jump or Call tests one of these pins and if appropriate, jumps to a new location. Otherwise, the instruction behaves like a NOP. These inputs are also connected to the status register bits S10 and S11 which may be read by the appropriate instruction (Figure 8).

User Outputs. The status register bits S5 and S6 connect directly to UO0 and UO1 pins and may be written to by the appropriate instruction. **Note:** the user output value is the inverse of the status register content.

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z89321 has three positive edge-triggered interrupt inputs. An interrupt is acknowledged at the end of an instruction execution. It takes two machine cycles to enter an interrupt instruction sequence. The PC is pushed onto the stack. A RET instruction transfers the contents of the stack to the PC and decrements the stack pointer by one word. The priority of the interrupts is INT0 = highest, INT2 = lowest. INT1 is dedicated to the CODEC interface and INT2 is dedicated to the 13-bit timer if both peripherals are enabled. **Note:** The SIEF instruction enables the interrupts. The SIEF instruction must be used before exiting an interrupt routine since the interrupts are automatically disabled when entering the routine.

Registers. The Z89321 has 19 physical internal registers and up to eight user-defined external registers. The EA2-EA0 determines the address of the external registers. The signals are used to read or write from the external registers /DS, WAIT, RD//WR..

I/O Bus. The processor provides a 16-bit, CMOS compatible bus. I/O Control pins provide convenient communication capabilities with external peripherals. Single cycle access is possible. For slower communications, an on-board hardware wait-state generator can be used to accommodate timing conflicts. Three latched I/O address pins are used to access external registers. EXT 4, 5, 6, 7 are used by the internal peripherals. Disabling a peripheral provides access to these addresses for general-purpose use.

CODEC Interface. The multi-compatible dual CODEC interface provides the necessary control signals for transmission of CODEC information to the DSP processor. The interface accommodates 8-bit PCM or 16-bit Linear CODECs. Special compatibility with Crystal Semiconductor's 4215/4216 CODEC provides the necessary interface for audio applications. Many general purpose 8-, 16-bit A/Ds, D/As are adaptable. The interface can also be used as a high-speed serial port.

μ-Law Compression. The 8-Bit CODEC interface mode provides μ-law compression from 13-bit format to 8-bit format. Decompression is performed in software by use of a 128 word look-up table.

Timer. Two programmable timers are available. One is dedicated to the CODEC interface, the other for general-purpose use. When a time-out event occurs, an interrupt request is generated. Single pass and or continuous modes are available. If the CODEC interface is not used, it is possible to use both timers for general purpose use.

Wait-State Generator. An internal wait-state generator is provided to accommodate slow external peripherals. A single wait-state can be implemented through control register EXT7-2. For additional states, a dedicated pin (WAIT) can be held high. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals (EXT bus).

REGISTERS

There are 19 internal registers which are defined below:

Register	Register Definition
P	Output of Multiplier, 24-bit
X	X Multiplier Input, 16-bit
Y	Y Multiplier Input, 16-bit
A	Accumulator, 24-bit
SR	Status Register, 16-bit
Pn:b	Six Ram Address Pointers, 8-bit each
PC	Program Counter, 16-bit
EXT4	13-Bit Timer Configuration Register
EXT5-1	CODEC Interface Channel 0 Data
EXT5-2	CODEC Interface Channel 0 Data
EXT6-1	CODEC Interface Channel 1 Data
EXT6-2	CODEC Interface Channel 1 Data
EXT7-1	CODEC Interface Configuration Register
EXT7-2	Wait-state generator/CODEC Interface Configuration Register

The following are virtual registers as physical RAM does not exist on the chip.

Register	Register Definition
EXTn	External Registers, 16-bit
BUS	D-Bus
Dn:b	Eight Data Pointers*

* Occupy the first four locations in RAM bank.

P holds the result of multiplications and is read-only.

X and **Y** are two 16-bit input registers for the multiplier. These registers can be utilized as temporary registers when the multiplier is not being used.

A is a 24-bit Accumulator. The output of the ALU is sent to this register. When 16-bit data is transferred into this register, is placed into the 16 MSB's and the least significant eight bits are set to zero. Only the upper 16 bits are transferred to the destination register when the Accumulator is selected as a source register in transfer instructions.

Pn:b are the pointer registers for accessing data RAM, (n = 0,1,2 refer to the pointer number) (b = 0,1 refers to RAM Bank 0 or 1). They can be directly read from or written to, and can point to locations in data RAM or Program Memory.

EXTn are external registers (n = 0 to 7). There are eight 16-bit registers here for mapping external devices into the address space of the processor. Note that the actual register RAM does not exist on the chip, but would exist as part of the external device such as an ADC result latch. Use of the CODEC interface and 13-bit timer reduces the number of external registers to four.

BUS is a read-only register which, when accessed, returns the contents of the D-Bus.

Dn:b refer to locations in RAM that can be used as a pointer to locations in program memory which is efficient for coefficient addressing. The programmer decides which location to choose from two bits in the status register and two bits in the operand. Thus, only the lower 16 possible locations in RAM can be specified. At any one time there are eight usable pointers, four per bank, and the four pointers are in consecutive locations in RAM. For example, if S3/S4 = 01 in the status register, then D0:0/D1:0/D2:0/D3:0 refer to register locations 4/5/6/7 in RAM Bank 0. Note that when the data pointers are being written to, a number is actually being loaded to Data RAM, so they can be used as a limited method for writing to RAM.

SR is the status register (Figure 8) which contains the ALU status and certain control bits (Table 8).

Table 8. Status Register Bit Functions

Status Register Bit	Function
S15 (N)	ALU Negative
S14 (OV)	ALU Overflow
S13 (Z)	ALU Zero
S12 (L)	Carry
S11 (UI1)	User Input 1
S10 (UI0)	User Input 0
S9 (SH3)	MPY Output Arithmetically Shifted Right by three bits
S8 (OP)	Overflow Protection
S7 (IE)	Interrupt Enable
S6 (UO1)	User Output 1
S5 (UO0)	User Output 0
S4-S3	"Short Form Direct" bits
S2-S0 (RPL)	RAM Pointer Loop Size

REGISTERS (Continued)

The status register may always be read in its entirety. S15-S10 are set/reset by the hardware and can only be read by software. S9-S0 can be written by software (Table 9).

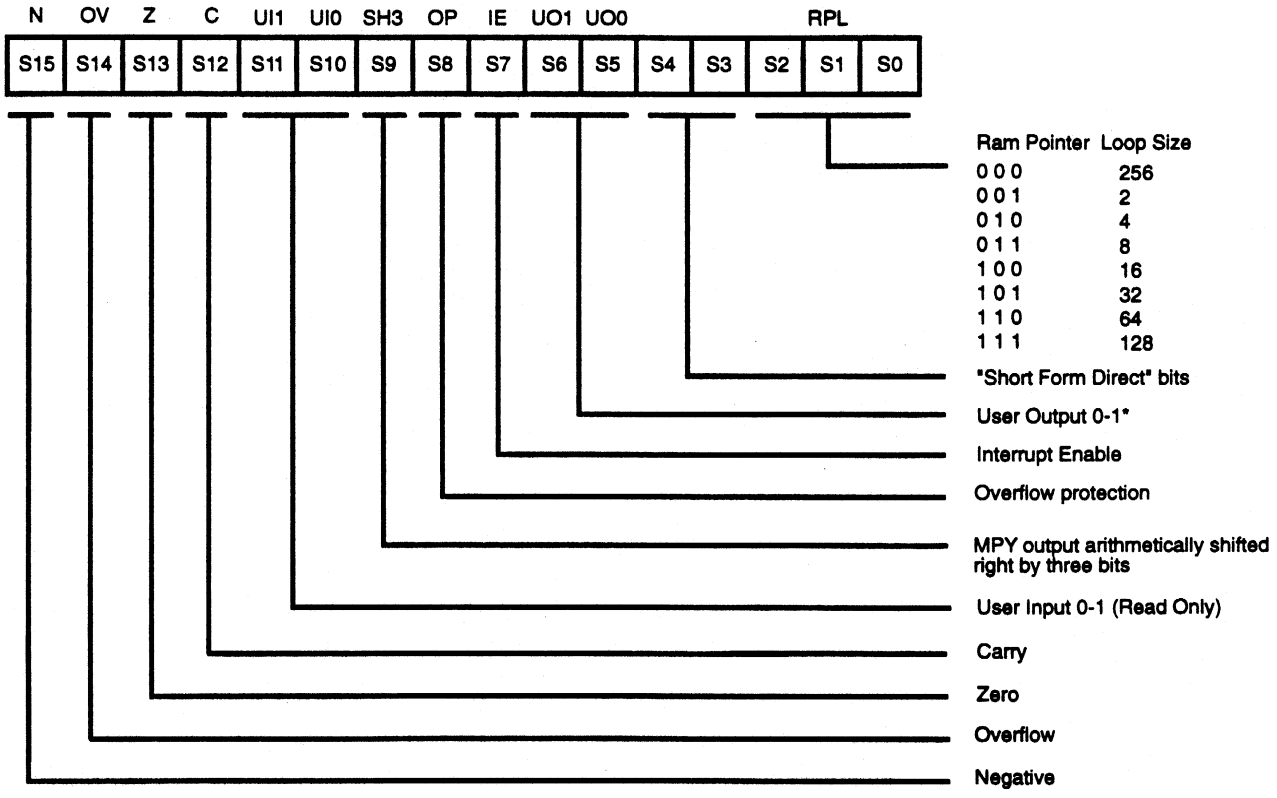
Table 9. RPL Description

S2	S1	S0	Loop Size
0	0	0	256
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

S15-S12 are set/reset by the ALU after an operation. S11-S10 are set/reset by the user inputs. S6-S0 are control bits described elsewhere. S7 enables interrupts. If S8 is set, the hardware clamps at maximum positive or negative values instead of overflowing. If S9 is set and a multiple/shift option is used, then the shifter shifts the result three bits right. This is used for scaling the data to prevent overflows

PC is the Program Counter. When this register is assigned as a destination register, one NOP machine cycle is added automatically to adjust the pipeline timing.

External Register, EXT4-EXT7 are used by the CODEC interface and 13-bit timer, the registers are reviewed in the CODEC interface section.



* The output value is the inverse of the status register content.

Figure 10. Status Register

PERIPHERALS

CODEC Interface

The CODEC Interface provides direct-connect capabilities for standard 8/16-bit CODECs. 8-bit PCM, 8-bit PCM with hardware μ-law conversion, 16-bit Linear and Crystal's Sigma-Delta Stereo CODEC modes are available. Registers are used to accommodate the CODEC Interface (EXT5, EXT6 and EXT7). The CODEC interface provides two Frame Sync signals, which allows two channels of data for transmission/receiving.

Note: μ-Law expansion must be done in software.

CODEC Interface Hardware

The Hardware for the CODEC Interface uses six 16-bit registers, μ-law compression logic and general purpose logic to control transfers to the appropriate register (Figure 10).

CODEC Interface Control Signals

SCLK (Serial Clock)

The Serial Clock provides a clock signal for operating the external CODEC. A 4-bit prescaler is used to determine the frequency of the output signal.

SCLK = (0.5* CLK)/PS where: CLK = System Clock
PS = 4-bit Prescaler*

Note: An internal divide-by-two is performed before the clock signal passed to the Serial Clock prescaler.

* The Prescaler is an up-counter.

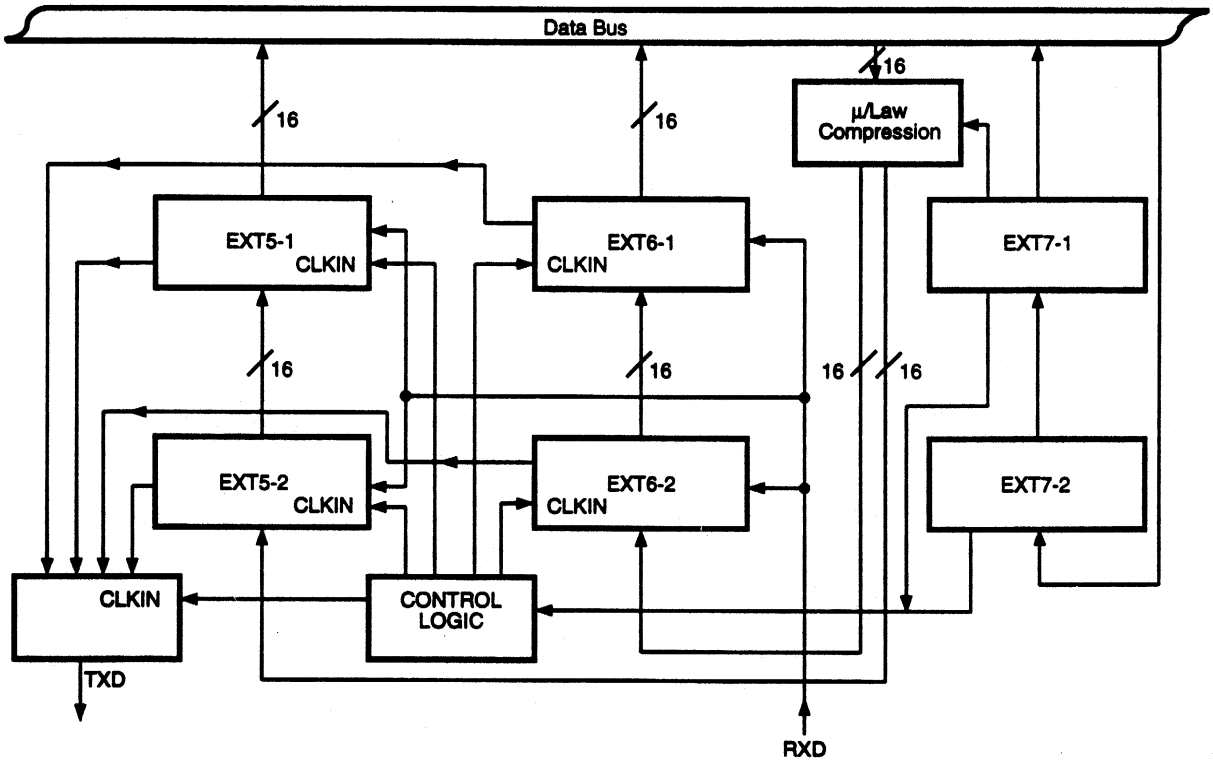


Figure 11. CODEC Interface Block Diagram

PERIPHERALS (Continued)

TXD (Serial Output to CODEC)
The TXD line provides 8, 16, and 64-bit data transfers. Each bit is clocked out of the processor by the rising edge of the SCLK. The MSB is transmitted first.

RXD (Serial Input from CODEC)
The RXD line provides 8, 16, and 64-bit data transfers. Each bit is clocked into the processor by the falling edge of the SCLK. The MSB is received first.

FS0, FS1 (Frame Sync)
The Frame Sync is used for enabling the transfer/receive of data. The rising and falling edge of the Frame Sync encloses the Serial data transmission.

Interrupt
Once the transmission of serial data is completed an internal interrupt signal is initiated. A single cycle low pulse provides an interrupt on INT1. The processor will jump to the defined Interrupt 1 vector location (see Figure 12).

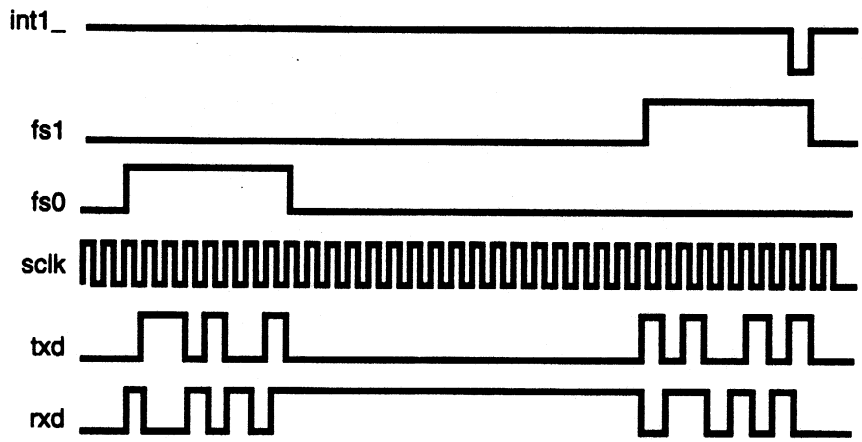


Figure 12. CODEC Interface Timing (8-Bit Mode)

CODEC Interface Timing

Figure 12 depicts a typical 8-bit serial data transfer using both of the CODEC Interface Channels. The transmitting data is clocked out on the rising edge of the SCLK signal. An external CODEC clocks data in on the falling edge of the SCLK signal. Once the serial data is transmitted, an interrupt is given. The CODEC Interface signals are not initiated if the CODEC Interface is not enabled.

The following modes are available for FSYNC and SCLK signals:

SCLK	FSYNC
Internal	Internal
External	External
External	Internal
Internal	External

The CODEC interface timing is independent of the Processor clock when external mode is chosen. This feature provides the capability for an external device to control the transfer of data to the Z89321. The Frame Sync signal envelopes the transmitted data (Figure 12), therefore care must be taken to ensure proper sync signal timing.

Full Duplex Operation

The Transmit and Receive lines are used for transfer of serial data to/from the CODEC interface. The CODEC interface performs both transmission and receiving of data at the same time. Figure 12 depicts transmission of 8-bit data.

Control Registers

The CODEC Interface is double-buffered, therefore four registers are provided for CODEC interface data storage. EXT5-1 and EXT5-2 operate with the Frame Sync 0 and EXT6-1 and EXT6-2 operate with Frame Sync 1. In 8- or 16-bit mode, the CODEC interface uses EXT5-1 and EXT6-1. For Stereo mode, all four registers are used. The configurations are shown in Figure 13 and Figure 14.

The CODEC Interface Control Register (EXT7-1) is shown in Figure 15. Setting of the CODEC mode, FSYNC, and Enable/Disable of CODEC 0 is done through this register. The wait-state generator, SCLK, and CODEC 1 is controlled from EXT7-2 (see Figure 14).

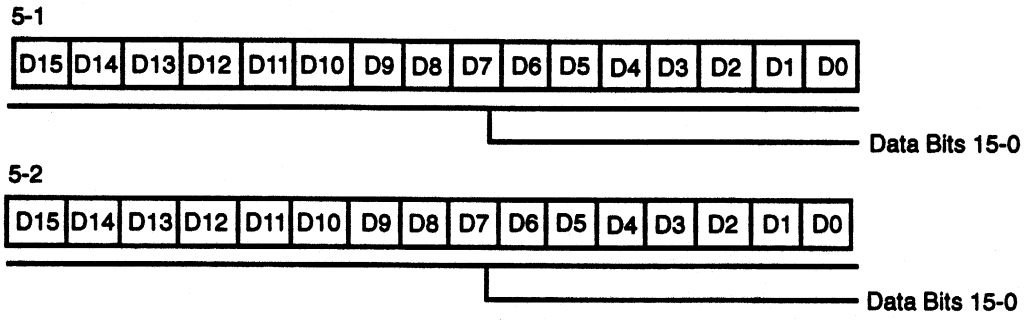


Figure 13. CODEC Interface Data Registers (Channel 0)

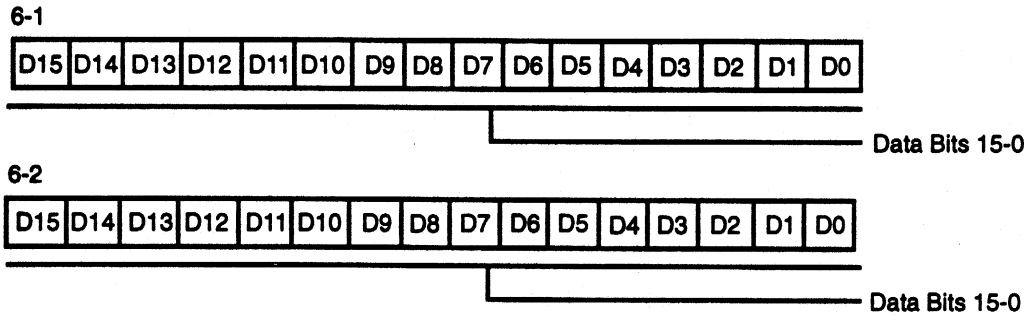


Figure 14. CODEC Interface Data Registers (Channel 1)

PERIPHERALS (Continued)

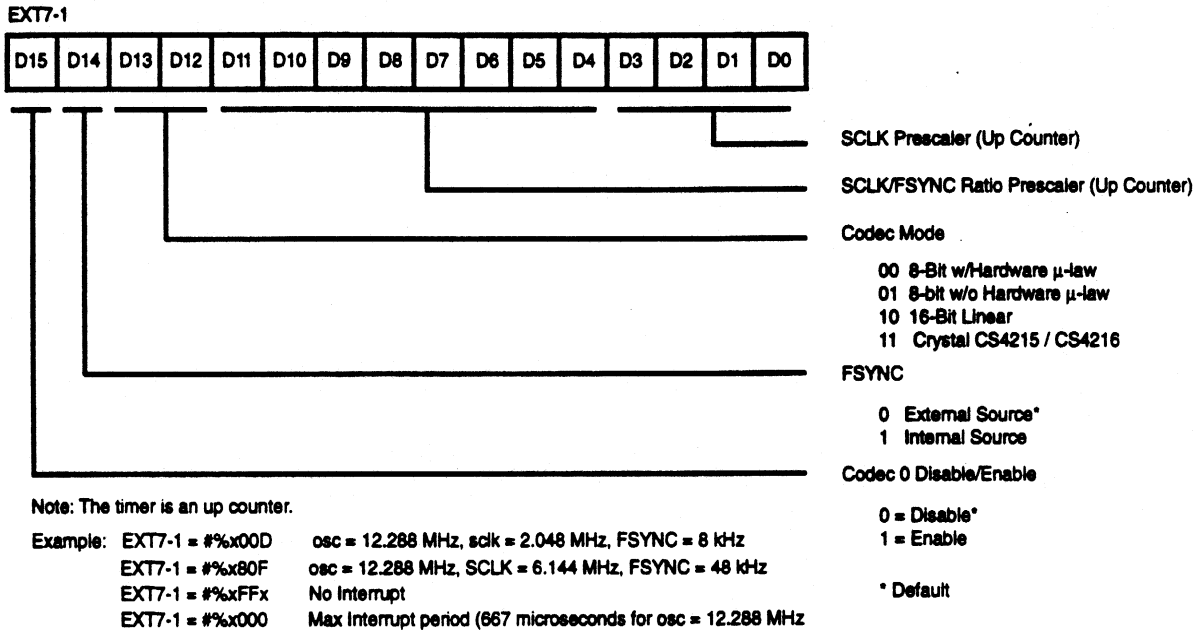


Figure 15. CODEC Interface Control Register

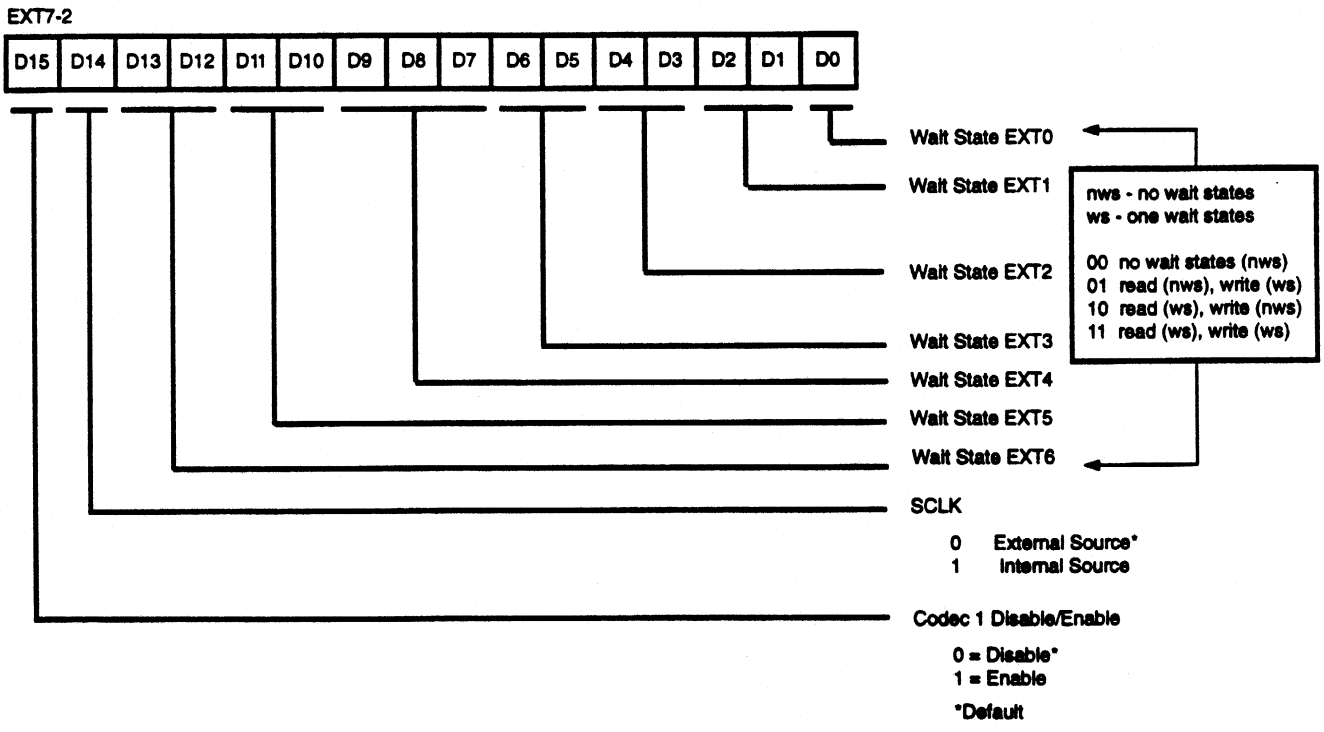


Figure 16. Wait-State/CODEC Interface Control Register

A/D Accommodation

The CODEC interface can be used for serial A/D or serial D/A transmission. The interface provides the necessary control signals to adapt to many standard serial convertors. The low-pass filter and smoothing filter is necessary for systems with converters.

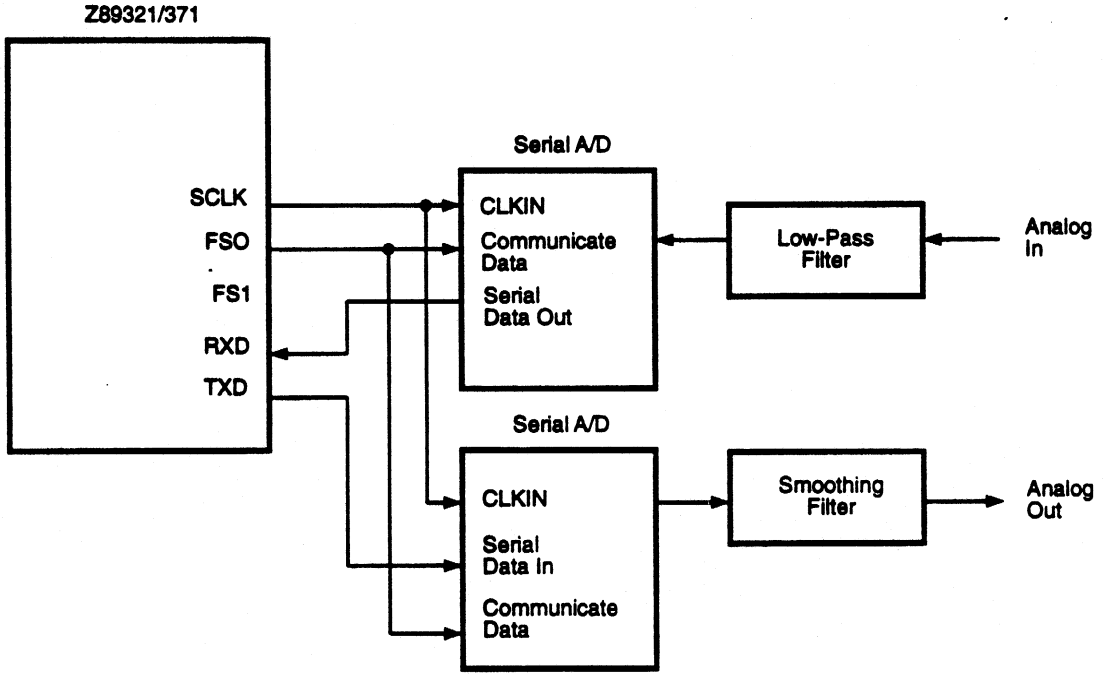


Figure 17. Block Diagram of A/D, D/A Implementation

High-Speed Serial Port

The Z89321 CODEC Interface can be used as a high-speed serial port. The necessary control signals are provided for adaptation to standard processors or external peripherals. Byte, word, or 64-bit data can be transmitted at speeds up to 10 Mbps. (Condition includes a 20 MHz oscillator. Data can be transferred with single cycle instructions to internal register file.)

Table 10. Tabulated Transmission Rates[1]

Transmission	Rate
Maximum SCLK	10 Mbps
Maximum Frame Sync	
8-bit	769.2 kHz
16-bit	476.2 kHz
Stereo (64 bit)	263.2 kHz

Notes:
[1] Calculations consider the interrupt access time (typically 4 cycles), transfer of data, loading of new data, and latency periods between CODEC transfers. During the interrupt cycle, developers often execute additional software, affecting the maximum transfer rate. Calculations are for single channel transfers only.

PERIPHERALS (Continued)

8-Bit CODEC Interface

The Z89321 provides an option for a standard 8-bit CODEC interface. Hardware μ-law compression is available (expansion performed by software look-up table). The CODEC interface transmits data consisting of 8-bit or compounded 8-bit information. Figure 18 shows a typical schematic arrangement.

The timing for this type of arrangement is presented in Figure 19. The flexible design provides adaptation for 16-bit linear CODEC.

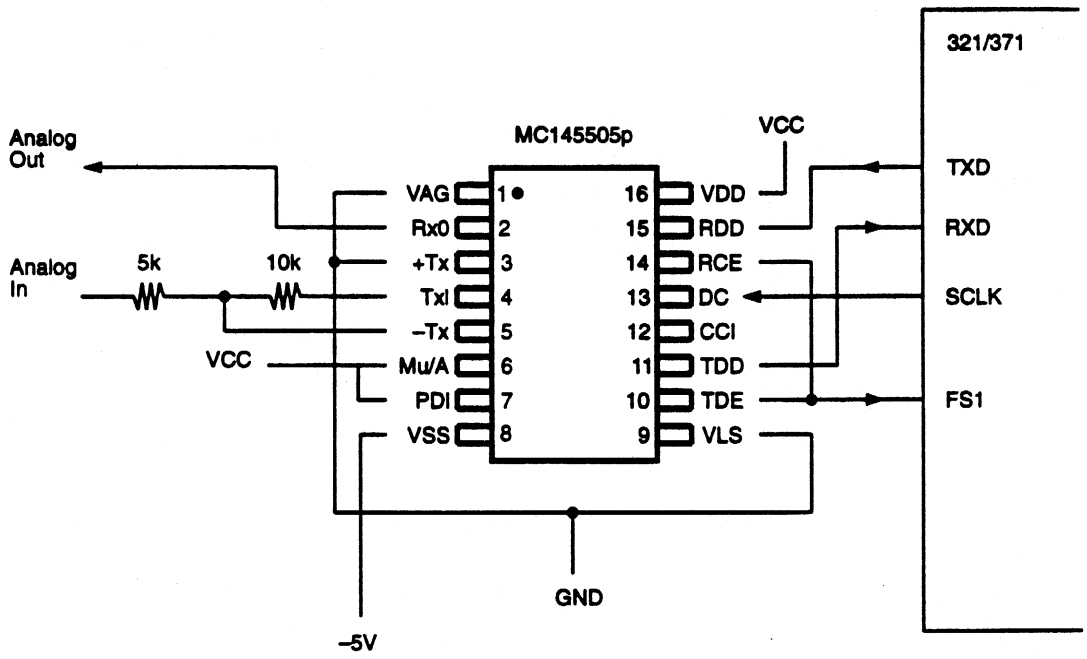


Figure 18. 8-Bit CODEC Schematic

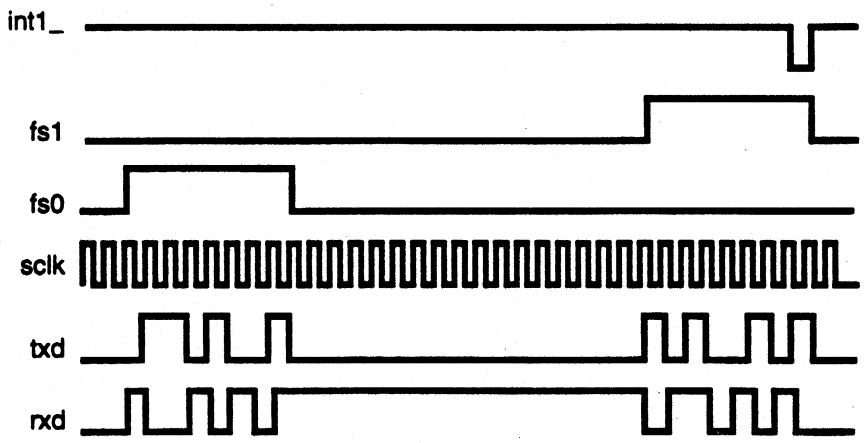


Figure 19. 8-Bit Mode Timing Diagram

16-Bit Linear CODEC Interface

For higher precision transmissions, a 16-bit linear CODEC is used. Data is not compressed in this mode of transmission. The Z89321 provides accommodation for two channels of 16-bit transmission. Figure 20 provides the timing for this option. For data acquisition systems, designers may opt for a 16-bit serial A/D. Figure 21 is a block diagram connection of the Z89321 with the AD1876 16-bit 100 kSPS Sampling ADC.

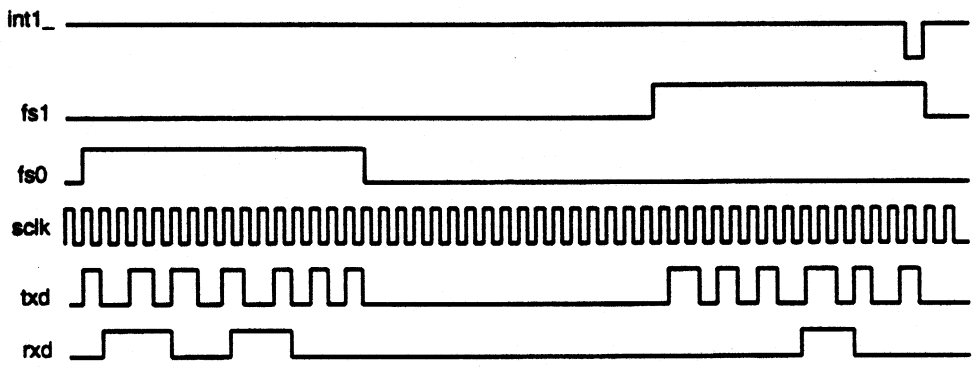


Figure 20. Timing Diagram (16-Bit Mode)

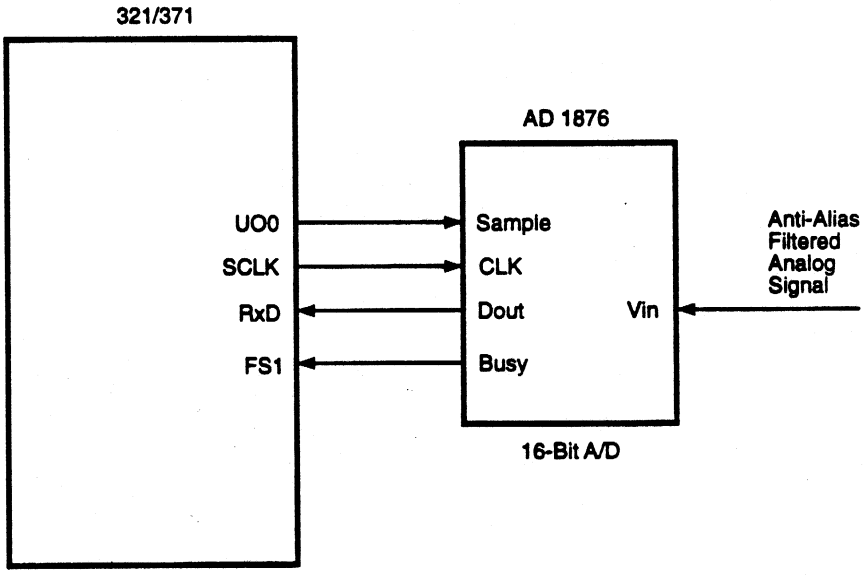


Figure 21. 16-Bit Serial A/D

PERIPHERALS (Continued)

Stereo CODEC Interface

The Z89321/371 adapts to the Crystal Semi CS4215 and CS4216 Stereo CODECs. The Z89321/371 CODEC interface provides direct connection to the CODECs for master or slave modes. Transmission of 64 bits of data (16 bits right channel, 16 bits left channel, and 32 bits of configuration information). This configuration information consists of input gain, input MUX, output attenuation, ADC clipping, and mute and error functions of the CODECs. Figure 22 shows a typical diagram of the CS4216 and the Z89321/371.

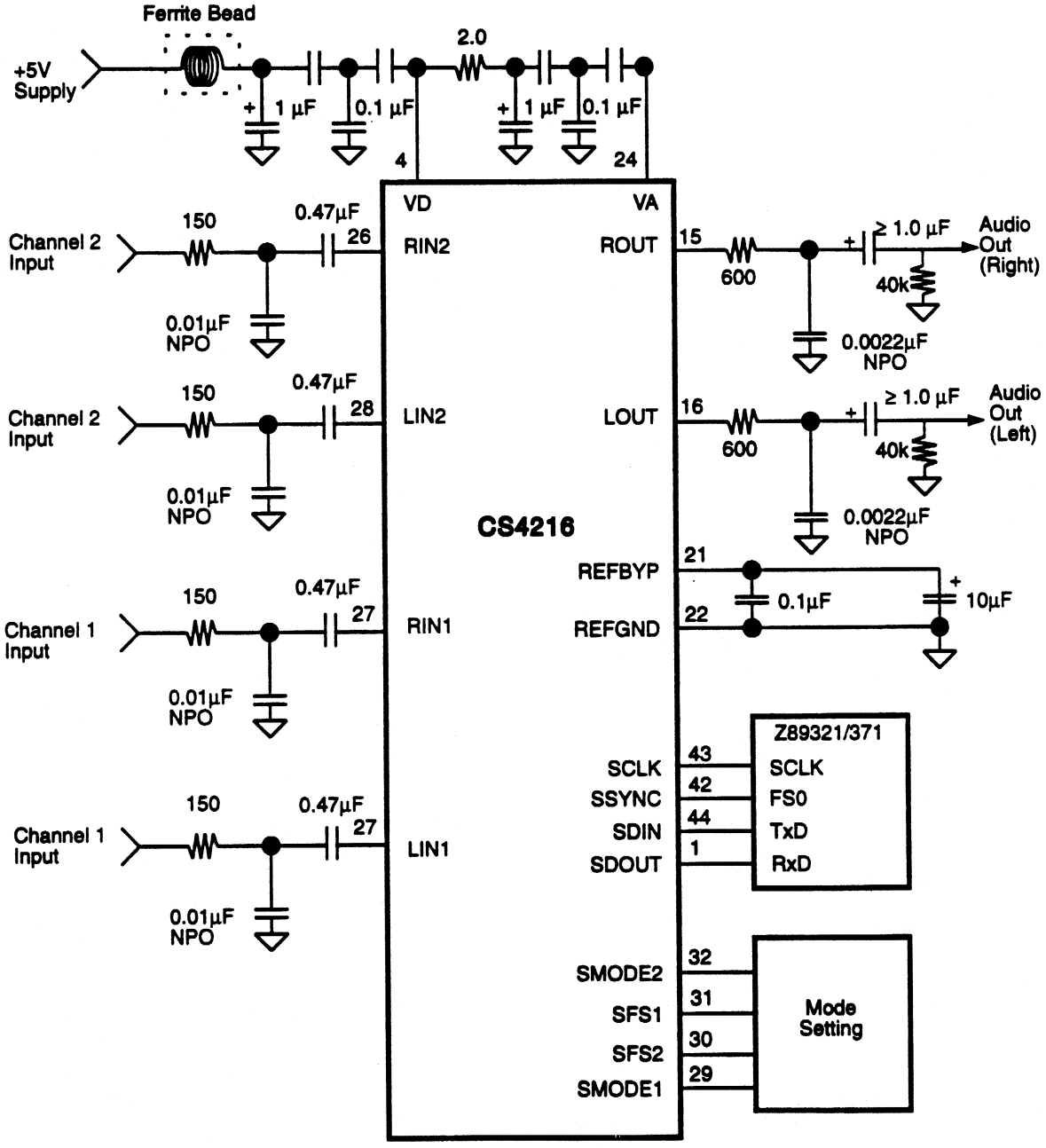


Figure 22. CS4216 Typical Schematic

The 64 bits of data transferred from the CODEC is placed in four registers (EXT5-1, 5-2, 6-1, 6-2) of the Z89321. The timing diagram for the Z89321/371 in this mode is presented in Figure 23.

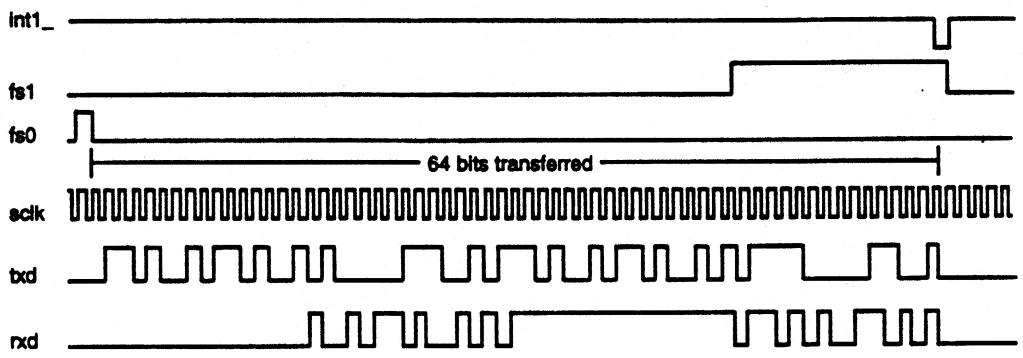


Figure 23. Timing Diagram (Stereo Mode)

13-Bit General-Purpose Timer

The 13-bit counter/timer is available for general-purpose use. When the counter counts down to the zero state, an interrupt is received on INT2. If the counter is disabled, EXT4 can be used as a general-purpose address. The counting operation of the counter can be disabled by resetting bit 14. Selection of the clock source provides the ability to extend the counter value past the 13 bits available in the control register. Use of the CODEC counter output can extend the counter to 26 bits (see Figure 24).

Notes:

Placing zeroes into the Count Value register does not generate an interrupt. Therefore it is possible to have a single-pass option by loading the counter with zero after the start of count.

The Counter is defaulted to the Enable state. If the system designer does not choose to use the timer, the counter can be disabled. Once disabled, the designer cannot enable the counter unless a reset of the processor is performed.

Example:

```
LD   EXT, #%C008    ;1100 0000 0000 1000
                    ; Enable Counter
                    ; Enable Counting
                    ; Clock Source = OSC/2
                    ; Count Value = 1000 = 8
                    ; Interrupt will occur every
                      16 clock cycles
```

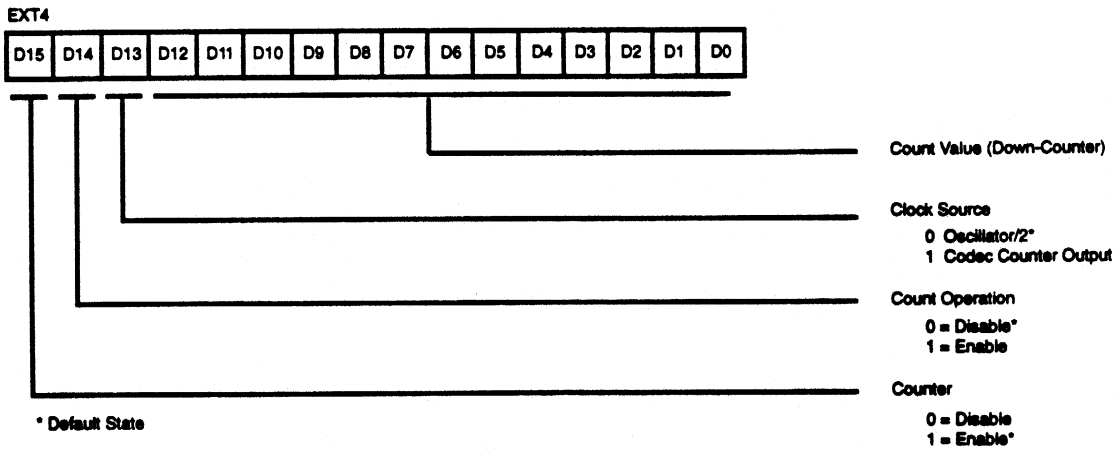


Figure 24. Timer Register

OPERATION

Disabling Peripherals

Disabling a peripheral (CODEC Interface, Counter) provides general-purpose use of the EXT address pertaining toward the specific peripheral. If the peripheral is not disabled, the EXT control signals and EXT data are still provided but transfer of data on the EXT pins is not available (since internal transfers are being processed on the internal bus). Care must be taken to ensure control of the EXT bus does not provide bus conflicts.

Reading Data from CODEC Interface*

External data is serially transferred into the CODEC interface registers from an external CODEC. This serial data is loaded into EXT5-2 (8- or 16-bit modes). Since the interface is double-buffered, data must be transferred to EXT5-1 before being transferred along the internal data bus of the processor. This is accomplished by writing data to EXT5-2.

Writing Data to CODEC Interface*

Internal data is transferred from the internal data bus of the processor to the EXT5-2 register. The CODEC interface constantly transfers and receives data during normal operation. Data to be transferred is loaded to EXT5-2 and is automatically serially transferred.

*EXT5-1 and EXT5-2 are used in the discussion. This information equally applies to EXT6-1 and EXT6-2 (see Figure 11 for CODEC Block Diagram).

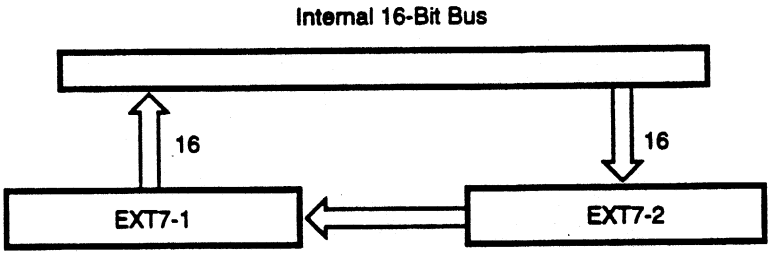


Figure 25. EXT7 Register Configuration

Loading EXT7

Since EXT7 is double-buffered, a pair of writes are performed when loading the EXT7 registers (see Figure 26).

LD EXT7, #%54F4	Loads CODEC Timer Register
LD EXT7, #%6CDA	Loads Wait-state Register
LD @P0:0, EXT7	Reads EXT7-1 and places data in RAM

Interrupt Availability

Three interrupts are provided on the Z89321. If all the peripherals are enabled, one general-purpose interrupt (INT0) is provided. The remaining interrupts are used as follows:

INT0	General-Purpose
INT1	CODEC Interface
INT2	13-bit timer

ADDRESSING MODES

This section discusses the syntax of the addressing modes supported by the DSP assembler. The symbolic name is used in the discussion of instruction syntax in the instruction descriptions.

Table 10. Addressing Modes

Symbolic Name	Syntax	Description
<pregs>	Pn:b	Pointer Register
<dregs> (Points to RAM)	Dn:b	Data Register
<hwregs>	X,Y,PC,SR,P EXTn,A,BUS	Hardware Registers
<accind> (Points to Program Memory)	@A	Accumulator Memory Indirect
<direct>	<expression>	Direct Address Expression
<limm>	#<const exp>	Long (16-bit) Immediate Value
<simm>	#<const exp>	Short (8-bit) Immediate Value
<regind> (Points to RAM)	@Pn:b @Pn:b+ @Pn:b–LOOP @Pn:b+LOOP	Pointer Register Indirect Pointer Register Indirect with Increment Pointer Register Indirect with Loop Decrement Pointer register Indirect with Loop Increment
<memind> (Points to Program Memory)	@@Pn:b @Dn:b @@Pn:b–LOOP @@Pn:b+LOOP @@Pn:b+	Pointer Register Memory Indirect Data Register Memory Indirect Pointer Register Memory Indirect with Loop Decrement Pointer Register Memory Indirect with Loop Increment Pointer Register Memory Indirect with Increment

ADDRESSING MODES (Continued)

There are eight distinct addressing modes for transfer of data (Figure 25 and Table 12).

<pregs>, <hwregs> These two modes are used for simple loads to and from registers within the chip such as loading to the Accumulator, or loading from a pointer register. The names of the registers need only be specified in the operand field. (Destination first then source.)

<regind> This mode is used for indirect accesses to the data RAM. The address of the RAM location is stored in the pointer. The "@" symbol indicates "indirect" and precedes the pointer, so @P1:1 tells the processor to read or write to a location in RAM1, which is specified by the value in the pointer.

<dregs> This mode is also used for accesses to the data RAM but only the lower 16 addresses in either bank. The 4-bit address comes from the status register and the operand field of the data pointer. Note that data registers are typically used not for addressing RAM, but loading data from program memory space.

<memind> This mode is used for indirect, indirect accesses to the program memory. The address of the memory is located in a RAM location, which is specified by the value in a pointer. So @@P1:1 tells the processor to read (write is not possible) from a location in memory, which is specified by a value in RAM, and the location of the RAM is in turn specified by the value in the pointer. Note that the data pointer can also be used for a memory access in this manner, but only one "@" precedes the pointer. In both cases the memory address stored in RAM is incremented by one each time the addressing mode is used to allow easy transfer of sequential data from program memory.

<accind> Similar to the previous mode, the address for the program memory read is stored in the Accumulator. @A in the second operand field loads the number in memory specified by the address in A.

<direct> The direct mode allows read or write to data RAM from the Accumulator by specifying the absolute address of the RAM in the operand of the instruction. A number between 0 and 255 indicates a location in RAM0, and a number between 256 and 511 indicates a location in RAM1.

<limm> This indicates a long immediate load. A 16-bit word can be copied directly from the operand into the specified register or memory.

<simm> This can only be used for immediate transfer of 8-bit data in the operand to the specified RAM pointer.

CONDITION CODES

The following defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one of its addressing modes, the instruction will only execute if the condition is true.

Name	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	Not Interrupts Enabled
NOV	Not Overflow
NU0	Not User Zero

Name	Description
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

INSTRUCTION DESCRIPTIONS

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
ABS	Absolute Value	ABS[<cc>,]<src>	<cc>,A	1	1	ABS NC,A
			A	1	1	ABS A
ADD	Addition	ADD<dest>,<src>	A,<pregs>	1	1	ADD A,P0:0
			A,<dregs>	1	1	ADD A,D0:0
			A,<limm>	2	2	ADD A,#%1234
			A,<memind>	1	3	ADD A,@@P0:0
			A,<direct>	1	1	ADD A,%F2
			A,<regind>	1	1	ADD A,@P1:1
			A,<hwregs>	1	1	ADD A,X
			A, <simm>			ADD A, #%12
AND	Bitwise AND	AND<dest>,<src>	A,<pregs>	1	1	AND A,P2:0
			A,<dregs>	1	1	AND A,D0:1
			A,<limm>	2	2	AND A,#%1234
			A,<memind>	1	3	AND A,@@P1:0
			A,<direct>	1	1	AND A,%2C
			A,<regind>	1	1	AND A,@P1:2+LOOP
			A,<hwregs>	1	1	AND A,EXT3
			A, <simm>			AND A, #%12
CALL	Subroutine call	CALL [<cc>,]<address>	<cc>,<direct>	2	2	CALL Z,sub2
			<direct>	2	2	CALL sub1
CCF	Clear carry flag	CCF	None	1	1	CCF
CIEF	Clear Carry Flag	CIEF	None	1	1	CIEF
COPF	Clear OP flag	COPF	None	1	1	COPF
CP	Comparison	CP<src1>,<src2>	A,<pregs>	1	1	CP A,P0:0
			A,<dregs>	1	1	CP A,D3:1
			A,<memind>	1	3	CP A,@@P0:1
			A,<direct>	1	1	CP A,%FF
			A,<regind>	1	1	CP A,@P2:1+
			A,<hwregs>	1	1	CP A,STACK
			A<limm>	2	2	CP A,#%FFCF
			A, <simm>			CP A, #%12
DEC	Decrement	DEC [<cc>,]<dest>	<cc>A,	1	1	DEC NZ,A
			A	1	1	DEC A
INC	Increment	INC [<cc>,] <dest>	<cc>,A	1	1	INC PL,A
			A	1	1	INC A
JP	Jump	JP [<cc>,]<address>	<cc>,<direct>	2	2	JP NIE,Label
			<direct>	2	2	JP Label

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
LD	Load destination with source	LD<dest>,<src>	A,<hwregs>	1	1	LD A,X
			A,<dregs>	1	1	LD A,D0:0
			A,<pregs>	1	1	LD A,P0:1
			A,<regind>	1	1	LD A,@P1:1
			A,<memind>	1	3	LD A,@D0:0
			A,<direct>	1	1	LD A,124
			<direct>,A	1	1	LD 124,A
			<dregs>,<hwregs>	1	1	LD D0:0,EXT7
			<pregs>,<simm>	1	1	LD P1:1,#%FA
			<pregs>,<hwregs>	1	1	LD P1:1,EXT1
			<regind>,<limm>	1	1	LD@P1:1,#1234
			<regind>,<hwregs>	1	1	LD @P1:1+,X
			<hwregs>,<pregs>	1	1	LD Y,P0:0
			<hwregs>,<dregs>	1	1	LD SR,D0:0
			<hwregs>,<limm>	2	2	LD PC,#%1234
			<hwregs>,<accind>	1	3	LD X,@A
			<hwregs>,<memind>	1	3	LD Y,@D0:0
			<hwregs>,<regind>	1	1	LD A,@P0:0–LOOP
			<hwregs>,<hwregs>	1	1	LD X,EXT6
			Note: When <dest> is <hwregs>, <dest> cannot be P.			
			Note: When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR.			
			Note: When <src> is <accind> <dest> cannot be A.			
MLD	Multiply	MLD<src1>,<src1>[,<bank switch>]	<hwregs>,<regind>	1	1	MLD A,@P0:0+LOOP
			<hwregs>,<regind>,<bank switch>	1	1	MLD A,@P1:0,OFF
			<regind>,<regind>	1	1	MLD @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MLD @P0:1,@P1:0,ON
			Note: If src1 is <regind> it must be a bank 1 register. Src2's <regind must be a bank 0 register.			
			Note: <hwregs> for src1 cannot be X.			
			Note: For the operands <hwregs>, <regind> the <band switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.			
MPYA	Multiply and add	MPYA <src1>,<src2>[,<bank switch>]	<hwregs>,<regind>	1	1	MPYA A,@P0:0
			<hwregs>,<regind>,<bank switch>	1	1	MPYA A,@P1:0,OFF
			<regind>,<regind>	1	1	MPYA @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MPYA@P0:1,@P1:0,ON
			Note: If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.			
			Note: <hwregs> for src1 cannot be X.			
			Note: For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.			

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MPYS	Multiply and subtract	MPYS<src1>,<src2>[,<bank switch>]	<hwregs>,<regind>	1	1	MPYS A,@P0:0
			<hwregs>,<regind>,<bank switch>	1	1	MPYS A,@P1:0,OFF
			<regind>,<regind>	1	1	MPYS @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MPYS@P0:1,@P1:0,ON
			Note: If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.			
			Note: <hwregs> for src1 cannot be X.			
			Note: For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON.			
NEG	Negate	NEG <cc>,A	<cc>, A	1	1	NEG MI,A
			A	1	1	NEG A
NOP	No operation	NOP	None	1	1	NOP
OR	Bitwise OR	OR <dest>,<src>	A, <pregs>	1	1	OR A,P0:1
			A, <dregs>	1	1	OR A, D0:1
			A, <limm>	2	2	OR A,#%2C21
			A, <memind>	1	3	OR A,@@P2:1+
			A, <direct>	1	1	OR A, %2C
			A, <regind>	1	1	OR A,@P1:0–LOOP
			A, <hwregs>	1	1	OR A,EXT6
			A, <simm>			OR A,#%12
POP	Pop value from stack	POP <dest>	<pregs>	1	1	POP P0:0
			<dregs>	1	1	POP D0:1
			<regind>	1	1	POP @P0:0
			<hwregs>	1	1	POP A
PUSH	Push value onto stack	PUSH <src>	<pregs>	1	1	PUSH P0:0
			<dregs>	1	1	PUSH D0:1
			<regind>	1	1	PUSH @P0:0
			<hwregs>	1	1	PUSH BUS
			<limm>	2	2	PUSH #12345
			<accind>	1	3	PUSH @A
			<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine	RET	None	1	2	RET
RL	Rotate Left	RL <cc>,A	<cc>,A	1	1	RL NZ,A
			A	1	1	RL A
RR	Rotate Right	RR <cc>,A	<cc>,A	1	1	RR C,A
			A	1	1	RR A

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
SCF	Set C flag	SCF	None	1	1	SCF
SIEF	Set IE flag	SIEF	None	1	1	SIEF
SLL	Shift left logical	SLL	[<cc>,]A	1	1	SLL NZ,A
			A	1	1	SLL A
SOPF	Set OP flag	SOPF	None	1	1	SOPF
SRA	Shift right arithmetic	SRA<cc>,A	<cc>,A	1	1	SRA NZ,A
			A	1	1	SRA A
SUB	Subtract	SUB<dest>,<src>	A,<pregs>	1	1	SUB A,P1:1
			A,<dregs>	1	1	SUB A,D0:1
			A,<limm>	2	2	SUB A,#%2C2C
			A, <memind>	1	3	SUB A,@D0:1
			A, <direct>	1	1	SUB A,%15
			A, <regind>	1	1	SUB A,@P2:0–LOOP
			A, <hwregs>	1	1	SUB A,STACK
			A, <simm>			SUB A, #%12
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A, <pregs>	1	1	XOR A,P2:0
			A, <dregs>	1	1	XOR A,D0:1
			A, <limm>	2	2	XOR A,#13933
			A, <memind>	1	3	XOR A,@@P2:1+
			A, <direct>	1	1	XOR A,%2F
			A, <regind>	1	1	XOR A,@P2:0
			A, <hwregs>	1	1	XOR A,BUS
			A, <simm>			XOR A, #%12

Bank Switch Enumerations. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether a bank switch is set on or off. To more clearly represent this two keywords are used (ON and OFF) which state the direction of the switch. These keywords are referred to in the instruction descriptions through the <bank switch> symbol.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Max.	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 34).

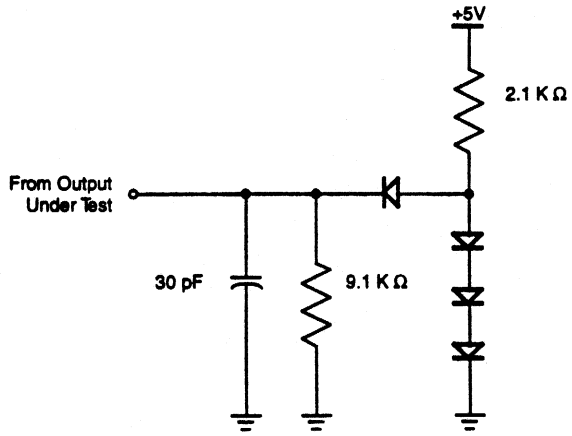


Figure 34. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, T_A = 0°C to +70°C unless otherwise specified)

Symbol	Parameter	Condition	Min.	Max.	Units
I_{DD}	Supply Current	V_{DD} = 5.5V fclock = 20 MHz [3]		60[1]	mA
I_{DC}	DC Power Consumption	V_{DD} = 5.5V	1	5	mA
V_{IH}	Input High Level		2.7		V
V_{IL}	Input Low Level			0.8	V
IL	Input Leakage			10	µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}–0.2		V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.5	V[2]
I_{FL}	Output Floating Leakage Current			10	µA

Notes:
[1] The Z89391 provides a typical I_{DD} of 70 mA.
[2] The followings specifications are pin specific.
EA0-2 has I_{OL} = 5 mA @ 0.5V
I_{OH} = 1 mA @ 3.0V
[3] The Z89371 operates to a maximum 16 MHz.

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V 10%, T_A = 0°C to +70°C unless otherwise specified)

Symbol	Parameter	Min (ns)	Max (ns)
Clock			
TCY	Clock Cycle Time	50 [1]	31250
Tr	Clock Rise Time		2
Tf	Clock Fall Time		2
CPW	Clock Pulse Width	25 [2]	
I/O			
DSVALID	/DS Valid Time from CLOCK Fall	0	15
DSHOLD	/DS Hold Time from CLOCK Rise	~~10~~ 0	15
EASET	EA Setup Time to /DS Fall	~~12~~ 10	
EAHOLD	EA Hold Time from /DS Rise	4	
RDSET	Data Read Setup Time to /DS Rise	~~14~~ 15	
RDHOLD	Data Read Hold Time from /DS Rise	~~6~~ 0	
WRVALID	Data Write Valid Time from /DS Fall		~~18~~ 5
WRHOLD	Data Write Hold Time from /DS Rise	~~5~~ 2	
Interrupt			
INTSET	Interrupt Setup Time to CLOCK Fall	7	
INTWIDTH	Interrupt Low Pulse Width	1 TCY	
Codec Interface			
SSET	SCLK Setup Time from Clock Rise		15
FSSET	FSYNC Setup Time from SCLK Rise		~~6~~ 7
TXSET	TXD Setup Time from SCLK Rise		7
RXSET	RXD Setup Time to SCLK Fall	7	
RXHOLD	RXD Hold Time from SCLK Fall	0	
Reset			
RRISE	Reset Rise Time		~~1000~~ 50
RSET	Reset Setup Time to CLOCK Rise	15	
RWIDTH	Interrupt Low Pulse Width	2 TCY	
ExternalProgram Memory			
PAVALID	PA Valid Time from CLOCK Rise		20
PDSET	PD Setup Time to CLOCK Rise	10	
PDHOLD	PD Hold Time from CLOCK Rise	10	
Wait State			
WSET	WAIT Setup Time to CLOCK Rise	~~23~~ 20	
WHOLD	WAIT Hold Time from CLOCK Rise	1 10	
Halt			
HSET	Halt Setup Time to CLOCK Rise	~~3~~ 4	
HHOLD	Halt Hold Time from CLOCK Rise	~~10~~ 12	

RWSET ≥ 10
RWHOLD ≥ 0

Notes:
[1] Z89371 TCY Min = 62.5 ns
[2] Z89371 CPW Min = 29 ns

TIMING DIAGRAMS

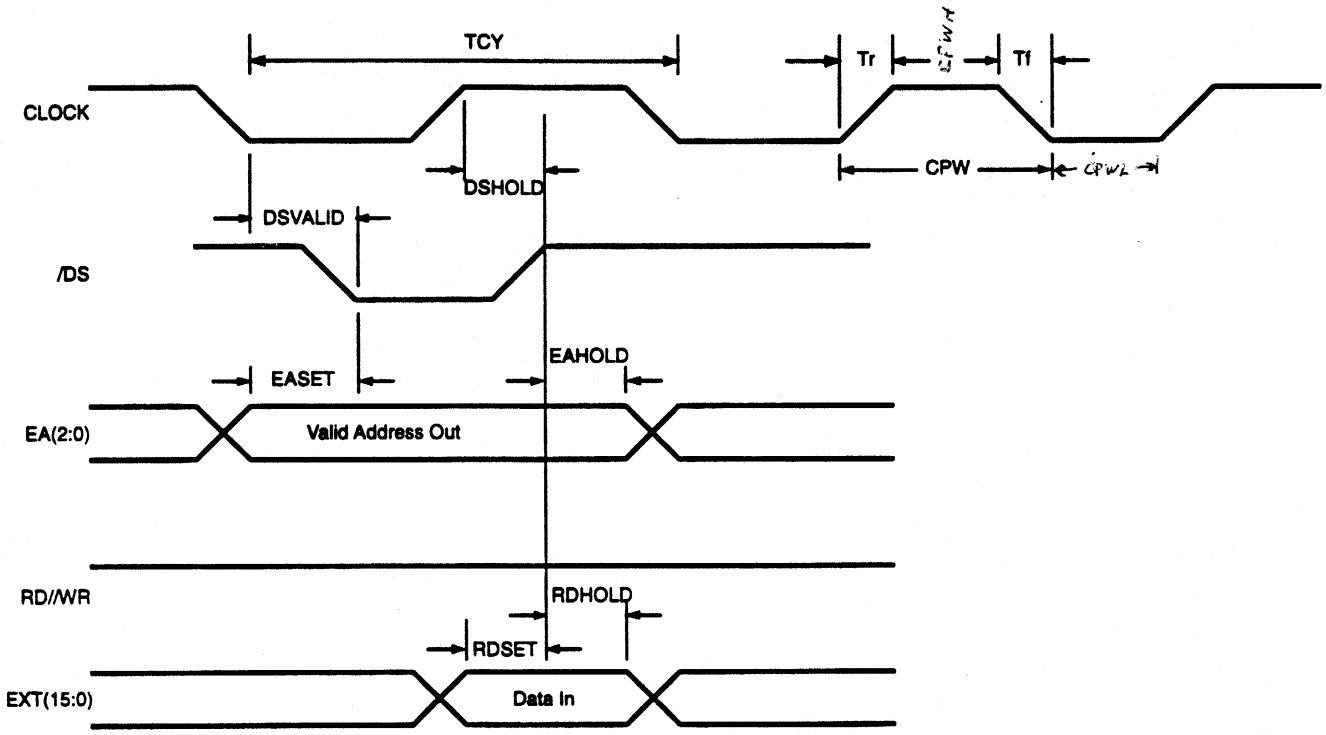


Figure 35. Read Timing Diagram

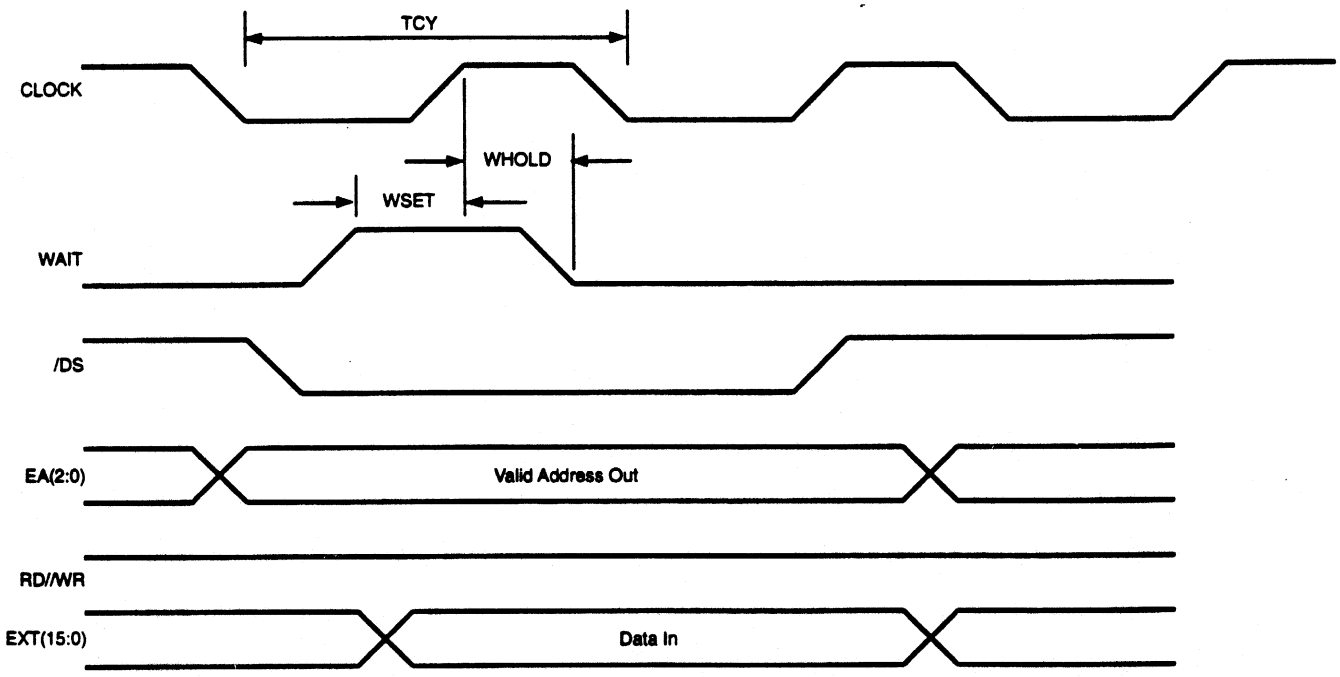


Figure 36. Read Timing Diagram Using WAIT Pin

TIMING DIAGRAMS (Continued)

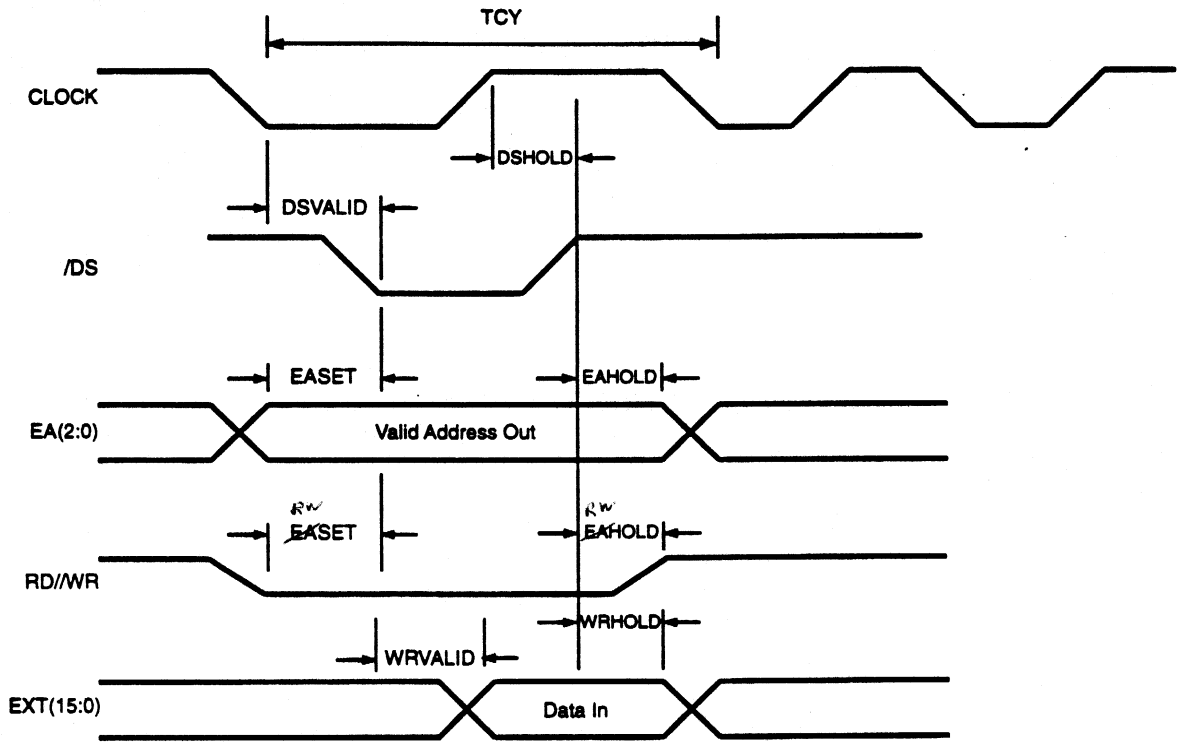


Figure 37. Write Timing Diagram

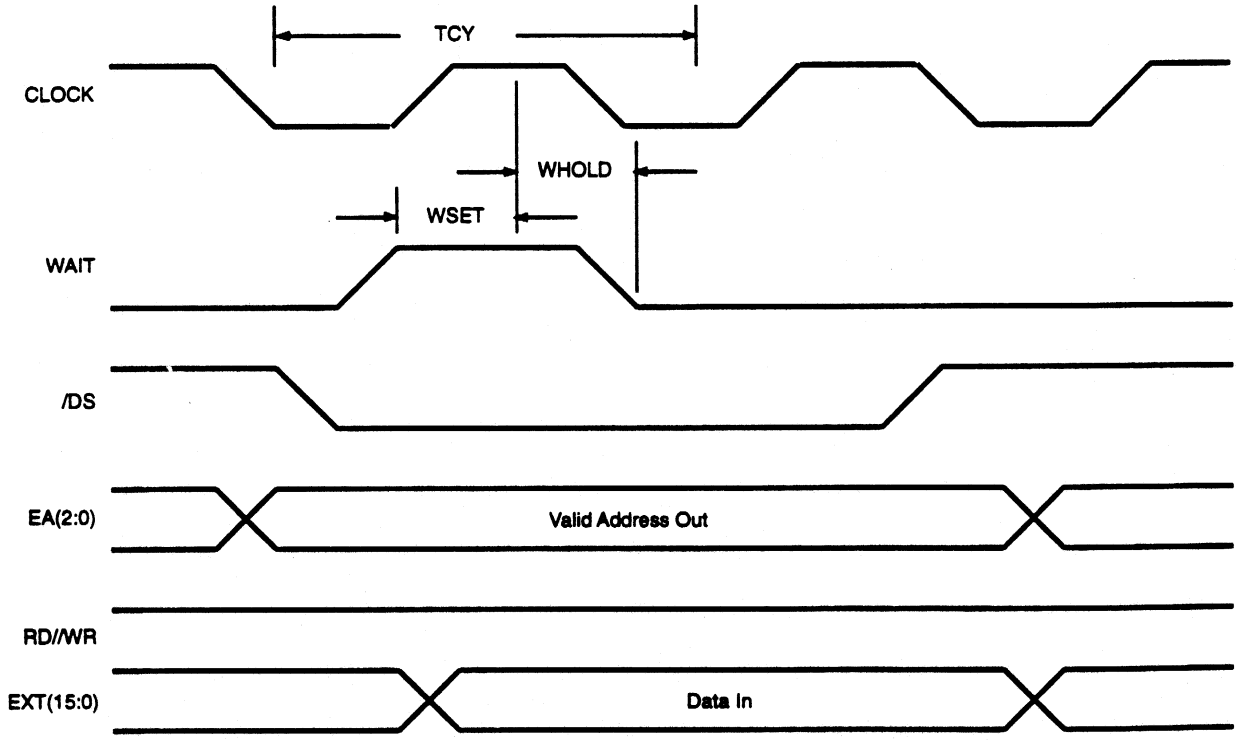


Figure 38. Write Timing Diagram Using WAIT Pin

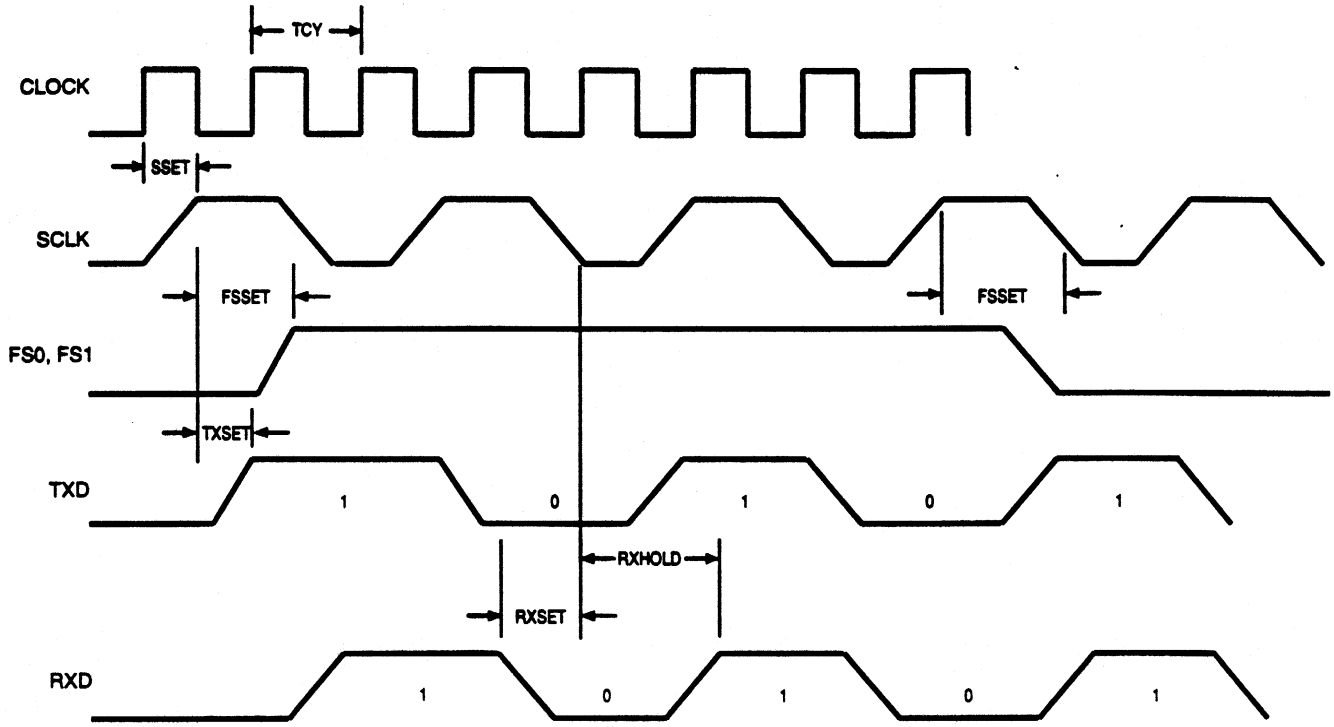


Figure 39. Codec Interface Timing Diagram

TIMING DIAGRAMS (Continued)

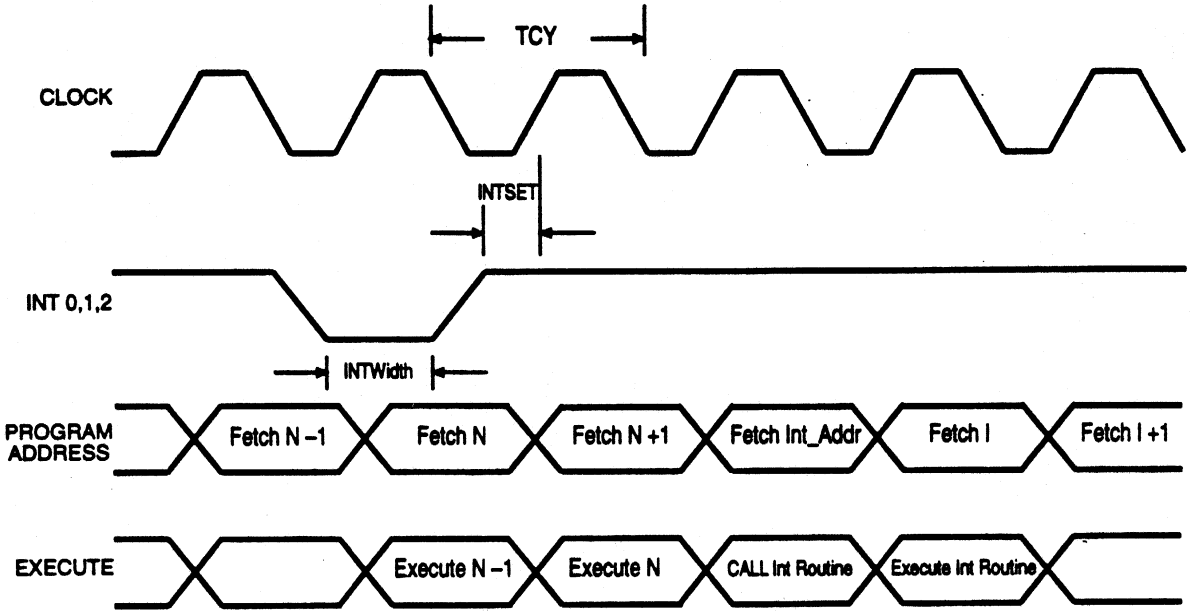


Figure 40. Interrupt Timing Diagram

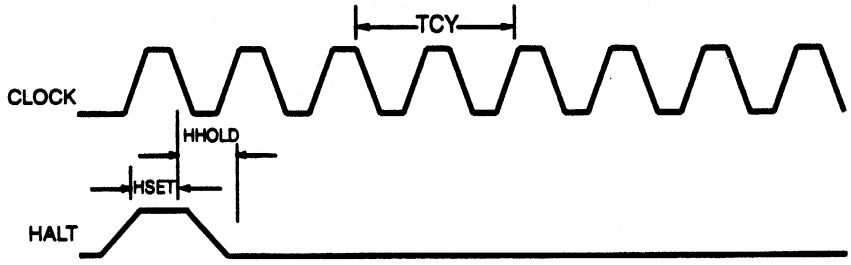
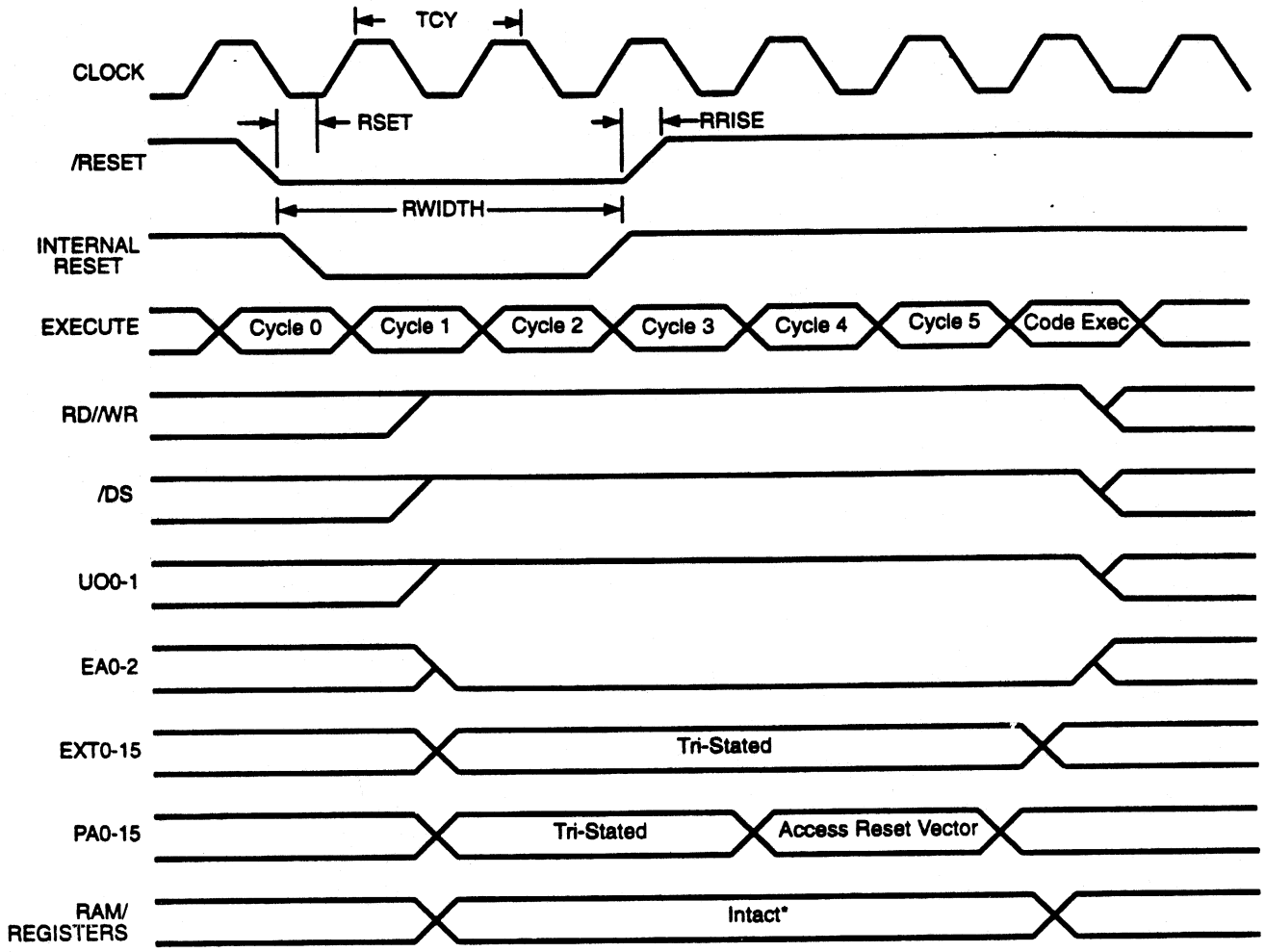


Figure 41. HALT Timing Diagram



* The RAM and hardware registers are left intact during a warm reset. A cold reset will produce random data in these locations. The status register is set to zeroes in both cases.

Figure 42. RESET Timing Diagram

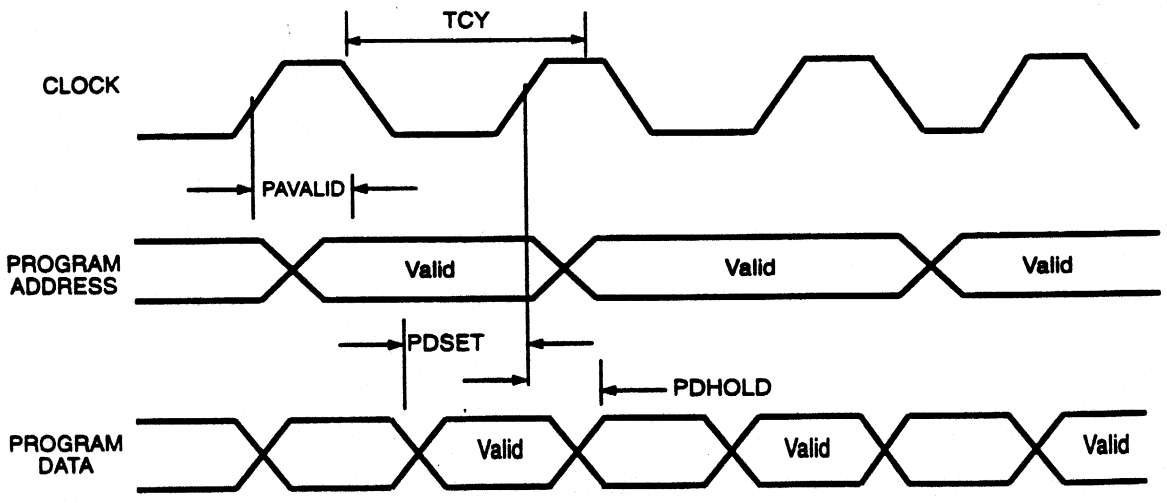
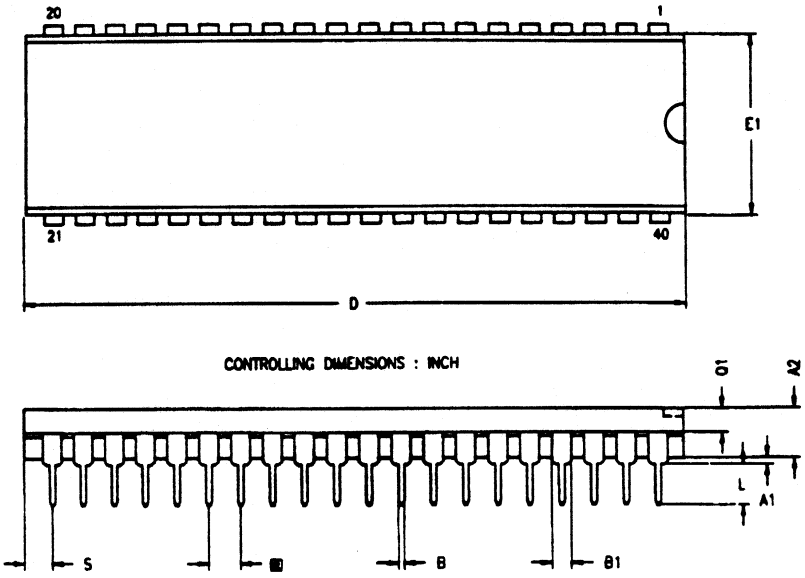
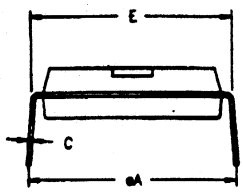


Figure 43. External Program Memory Port Timing Diagram

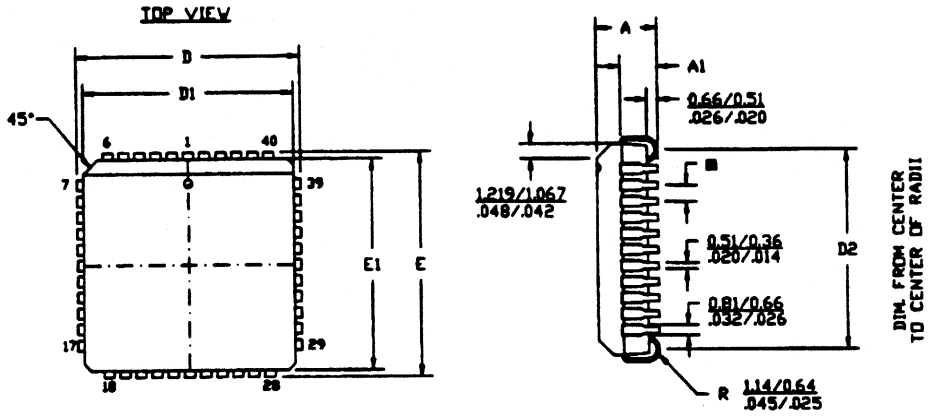
PACKAGE INFORMATION





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

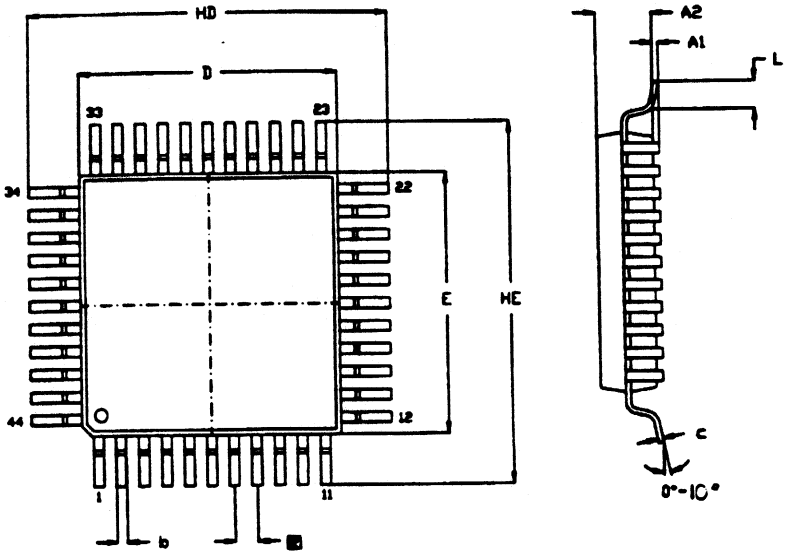
40-Pin DIP Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

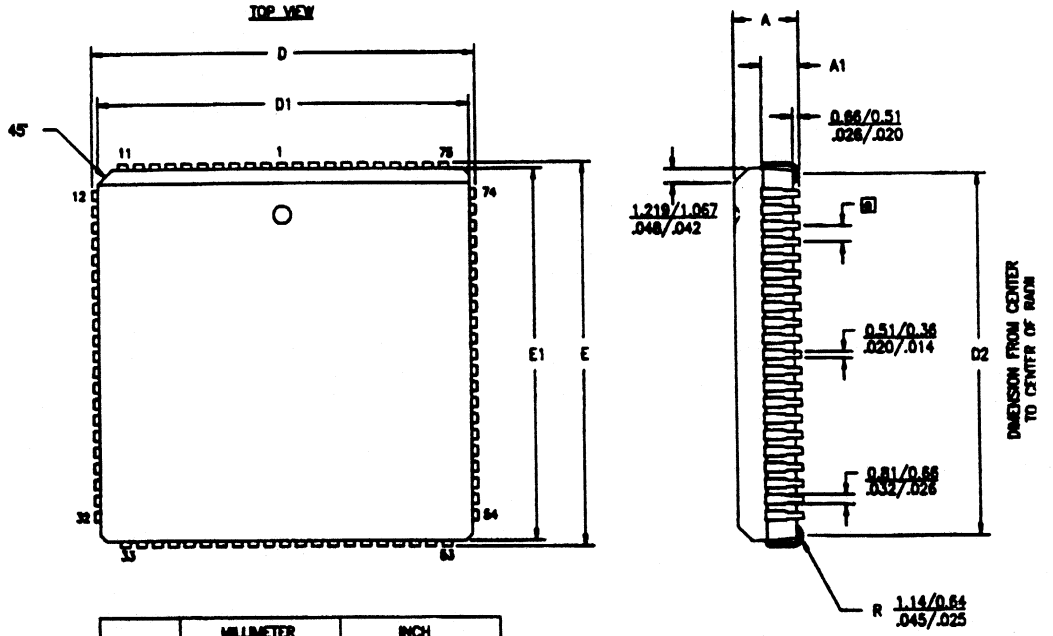
44-Lead PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

44-Pin QFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	30.10	30.35	1.185	1.195
D1/E1	29.21	29.41	1.150	1.158
D2	27.94	28.58	1.100	1.125
e	1.27 TYP		.050 TYP	

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

84-Pin PLCC Package Diagram

ORDERING INFORMATION

Z89321	Z89371	Z89391
20 MHz 44-Pin PLCC Z8932120VSC	**16 MHz** 44-pin PLCC Z8937116VSC	**20 MHz** 84-Pin PLCC Z8939120VSC
20 MHz 40-Pin DIP Z8932120PSC	**16 MHz** 40-pin DIP Z8937116PSC	
20 MHz 44-Pin QFP Z8932120FSC	**16 MHz** 44-pin QFP Z8937116FSC	

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P= Plastic DIP
V = Plastic PLCC
F = Plastic QFP

Temperature
S = 0°C to +70°C

Speed
20 = 20 MHz
16 = 16 MHz

Environmental
C = Plastic Standard

Example:

Z 89321 20 V S C is a Z89321, 20 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow